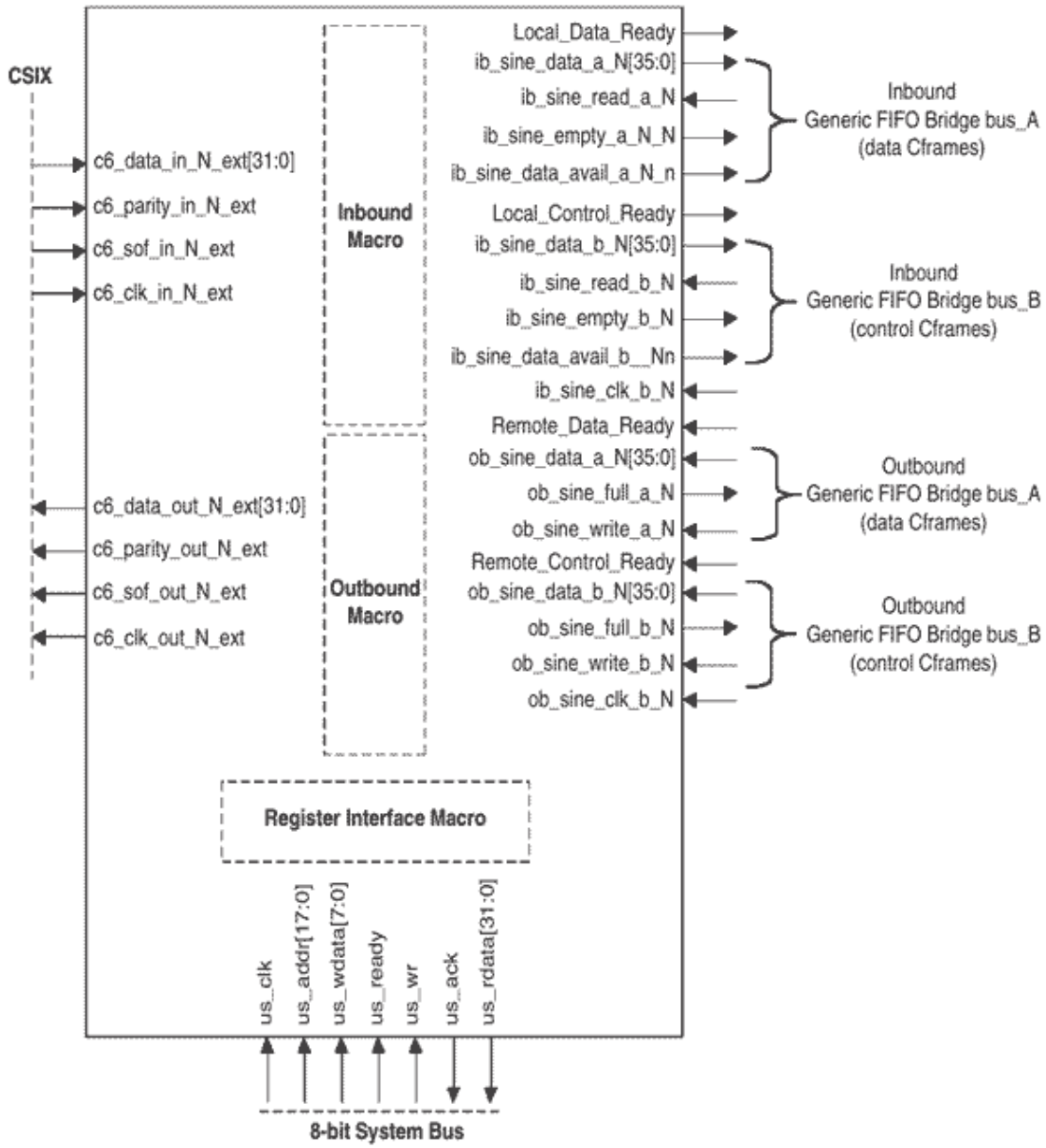
CSIX Level 1

Overview

As stated by the CSIX Forum, the CSIX standard defines the physical and message layers of the interconnect between traffic managers (TM) and the switching fabric. The CSIX interface is designed to support a wide variety of system architectures and markets; and provides a framework with a common set of mechanisms for enabling a fabric and a TM to communicate. This includes unicast addressing for up to 4096 fabric ports, and multiple traffic classes that isolate data going to the same fabric port. Link level flow control is in-band and broken into a data and a control queue to isolate traffic based on this granular type. Flow control between the fabric and TM is defined and is relative to both fabric port and class. Three multicast approaches are defined. The interface assumes cell segmentation in the TM, but allows compression of the transfer.

Lattice Semiconductor's CSIX Level 1 IP core links a compliant CSIX-L1 interface to Lattice's Generic FIFO Bridge interface (a simple FIFO interface). Inbound control and data frames from the CSIX port are deposited into the core's inbound FIFOs; CSIX frames stored in the core's outbound FIFOs are driven onto the outbound CSIX interface. The Generic FIFO Bridge interface directly accesses the core's inbound and outbound FIFOs.



Features

- Implements a CSIX-L1-to-Generic FIFO Bridge
- Supports 32-Bit, 100MHz CSIX-L1 Interface
- Up to Four Paramaterizable 32-bit Channel Instantiations
- Paramaterizable Channel Aggregation (32-Bit to 128-Bit)
- Paramaterizable FIFO Size (Up to 2048 Bytes)
- Programmable FIFO Thresholds
- Supports MAX_FRAME_PAYLOAD_SIZE from 1 to 256 Bytes
- Transports Unicast, Multicast, Broadcast, and Flow Control Frames
- Filters Idle Frames (Not Transported Through Core)
- Delineates Cframes at Generic FIFO Bridge Interface with Start/End Flags (SOF and EOF)
- Passes Entire CSIX Frame Structure Across Generic FIFO Bridge Interface
- Passes CSIX Link Level Control Directly to Generic FIFO Bridge (Bypasses FIFOs)
- Supports CSIX-L1 Link Layer Flow Control (XON/XOFF)
- Programmable Horizontal and Vertical Parity Check Enables
- Internal Register Set for Control and Status Management
- 8-Bit Register Interface Compatible with ORCA System Bus

Evaluation Configurations

Performance and Utilization for ORCA 4

Configuration Number	csix_lev1_o4_1_001.lpc (AMID 7956)
Core Description	one 32-bit csix
FIFO Size	1024
PFUs	222
LUTs	818
Regs	1198
EBRs	4
PIO	112
Buried Generic FIFO Bridge I/O	156
Buried Reg I/O	26
f_{MAX} (MHz)	100

Ordering Information

Part Numbers:

For ORCA 4: CSIX-LEV1-O4-N1

To find out how to purchase the CSIX Level 1 IP Core, please contact your **local Lattice Sales Office**.