

CY7C1081DV33

64-Mbit (4 M × 16) Static RAM

Features

- High speed □ t_{AA} = 12 ns
- Low active power □ I_{CC} = 300 mA at 12 ns
- Low complementary metal oxide semiconductor (CMOS) standby power
 I_{SB2} = 100 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with CE₁ and CE₂ features
- Available in Pb-free 48-ball fine ball grid array (FBGA) package

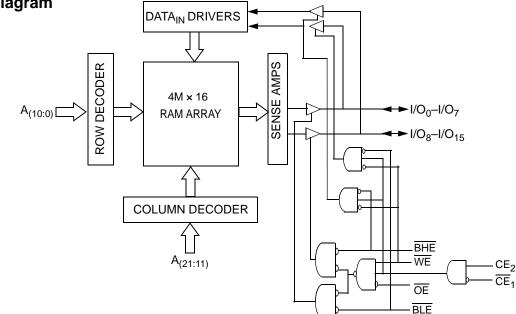
Functional Description

The CY7C1081DV33 is a high-performance CMOS static RAM organized as 4,194,304 words by 16 bits.

To write to the device, tak<u>e</u> Chip Enables (\overline{CE}_1 LOW and CE_2 <u>HIGH</u>) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₂₁). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₂₁).

To read from the device, tak<u>e</u> Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 9 for a complete description of read and write modes.

The input and output pins $(I/O_0 \text{ through } I/O_{15})$ are placed in a high impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE} \text{ HIGH}$), both byte high enable and byte low enable are disabled (BHE, BLE HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and WE LOW).



Logic Block Diagram

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CY7C1081DV33

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Selection Guide

Description	-12	Unit
Maximum access time	12	ns
Maximum operating current	300	mA
Maximum CMOS standby current	100	mA

Pin Configuration

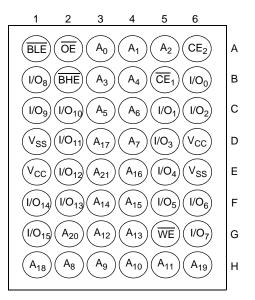


Figure 1. 48-Ball FBGA (Top View)



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied55 °C to +125 °C
Supply voltage on V _{CC} relative to GND $^{[1]}$ 0.5 V to +4.6 V
DC voltage applied to outputs
DC voltage applied to outputs in high-Z state ^[1] 0.5 V to V_{CC} + 0.5 V
DC input voltage ^[1] 0.5 V to V _{CC} + 0.5 V

Current into outputs (LOW)	20 mA
Static discharge voltage	>2001 V
(MIL-STD-883, Method 3015)	
Latch-up current	>140 mA

Operating Range

Range	Ambient Temperature	V _{cc}	Speed
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	12 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Unit		
Farameter	Description		Min	Max	onit	
V _{OH}	Output HIGH voltage	$V_{CC} = Min, I_{OH} = -4.0 \text{ mA}$	2.4	-	V	
V _{OL}	Output LOW voltage	$V_{CC} = Min, I_{OL} = 8.0 mA$	_	0.4	V	
V _{IH}	Input HIGH voltage		2.0	$V_{CC} + 0.3$	V	
V _{IL}	Input LOW voltage ^[1]		-0.3	0.8	V	
I _{IX}	Input leakage current	$GND \le V_{IN} \le V_{CC}$	-1	+1	μΑ	
I _{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output Disabled	-1	+1	μΑ	
I _{CC}	V _{CC} operating supply current	$V_{CC} = Max$, f = f _{max} = 1/t _{RC} , I _{OUT} = 0 mA CMOS levels	-	300	mA	
I _{SB1}	Automatic CE power-down current – TTL inputs	$ \begin{aligned} & \text{Max } V_{\text{CC}}, \ \overline{\text{CE}}_1 \geq \text{V}_{\text{IH}}, \ \text{CE}_2 \leq \text{V}_{\text{IL}}, \\ & \text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or } \text{V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \ \text{f} = \text{f}_{\text{max}} \end{aligned} $	-	120	mA	
I _{SB2}	Automatic CE power-down current – CMOS inputs	$ \begin{split} & Max\;V_{\mathrm{CC}}, \overline{\mathrm{CE}}_1 \geq V_{\mathrm{CC}} - 0.3\;V, CE_2 \leq 0.3\;V, \\ & V_{\mathrm{IN}} \geq V_{\mathrm{CC}} - 0.3\;V, or\;V_{\mathrm{IN}} \leq 0.3\;V, f = 0, \end{split} $	-	100	mA	

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	er Description Test Conditions		Max	Unit
C _{IN}	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 3.3 \text{ V}$	32	pF
C _{OUT}	I/O capacitance		40	pF

Thermal Resistance

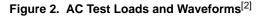
Tested initially and after any design or process changes that may affect these parameters.

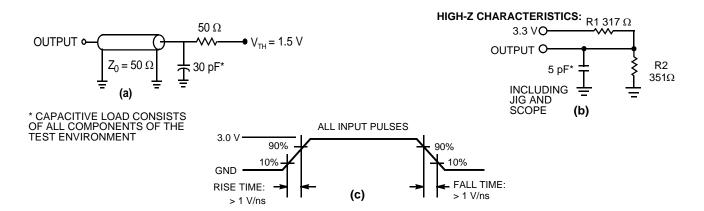
Parameter	ter Description Test Conditions		FBGA	Unit
JA		Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	55	°C/W
- 30	Thermal resistance (junction to case)		23.04	°C/W

Note

1. V_{IL} (min) = -2.0 V and V_{IH} (max) = V_{CC} + 2 V for pulse durations of less than 20 ns.





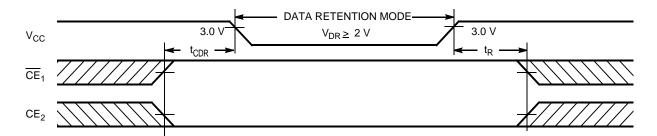


Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Тур	Max	Unit
V _{DR}	V _{CC} for data retention		2	-	-	V
I _{CCDR}	Data retention current	$\begin{split} & V_{CC} = 2 V, \overline{CE}_1 \geq V_{CC} - 0.2 V, CE_2 \leq 0.2 V, \\ & V_{IN} \geq V_{CC} - 0.2 V \text{ or } V_{IN} \leq 0.2 V \end{split}$	-	-	100	mA
t _{CDR} ^[3]	Chip deselect to data retention time		0	_	_	ns
t _R ^[4]	Operation recovery time		12	-	_	ns

Figure 3. Data Retention Waveform



Notes

- Valid SRAM operation does not occur until the power supplies reach the minimum operating V_{DD} (3.0 V). 100 μ s (t_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation begins to include reduction in V_{DD} to the data retention (V_{CCDR} , 2.0 V) voltage. Tested initially and after any design or process changes that may affect these parameters. 2.
- 3.
- 4. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) \ge 50 µs or stable at V_{CC}(min) \ge 50 µs.



AC Switching Characteristics

Over the Operating Range [5]

Devenuetor	Description	-	12	Unit
Parameter	Description	Min	Max	
Read Cycle				L
t _{power}	V _{CC} (typ) to the first access ^[6]	100	-	μS
t _{RC}	Read cycle time	12	-	ns
t _{AA}	Address to data valid	-	12	ns
t _{OHA}	Data hold from address change	3	-	ns
t _{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to Data Valid	-	12	ns
t _{DOE}	OE LOW to data valid	-	7	ns
t _{LZOE}	OE LOW to low-Z	1	-	ns
t _{HZOE}	OE HIGH to high-Z ^[7]	-	7	ns
t _{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to low-Z ^[7]	3	-	ns
t _{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to high-Z ^[7]	-	7	ns
t _{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up ^[8]	0	-	ns
t _{PD}	CE ₁ HIGH and CE ₂ LOW to power-down ^[8]	-	12	ns
t _{DBE}	Byte enable to data valid	-	7	ns
t _{LZBE}	Byte enable to low-Z	1	-	ns
t _{HZBE}	Byte disable to high-Z	-	7	ns
Write Cycle ^[9, 10]				
t _{WC}	Write cycle time	12	-	ns
t _{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	9	-	ns
t _{AW}	Address setup to write end	9	-	ns
t _{HA}	Address hold from write end	0	-	ns
t _{SA}	Address setup to write start	0	-	ns
t _{PWE}	WE pulse width	9	-	ns
t _{SD}	Data setup to write end	7	-	ns
t _{HD}	Data hold from write end	0	-	ns
t _{LZWE}	WE HIGH to low-Z ^[7]	3	-	ns
t _{HZWE}	WE LOW to high-Z ^[7]	-	7	ns
t _{BW}	Byte enable to end of write	9	-	ns

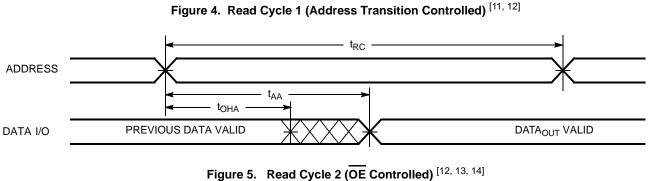
Notes

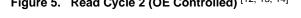
5. Test conditions are based on signal transition time of 3 ns or less and timing reference levels of 1.5 V and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of AC Test Loads and Waveforms^[2], unless specified otherwise.
6. t_{power} is the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
7. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms^[2].
8. These parameters are guaranteed by design and are not tested.
9. The internal memory write time is defined by the overlap of WE. CE₁ = V_{IL}, and CE₂ = V_{IH}. Chip enables must be active and WE and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
10. The minimum write order to the first Quele 2 (WE controlled, QE LOW) is the sum of the set of the sum of the set.

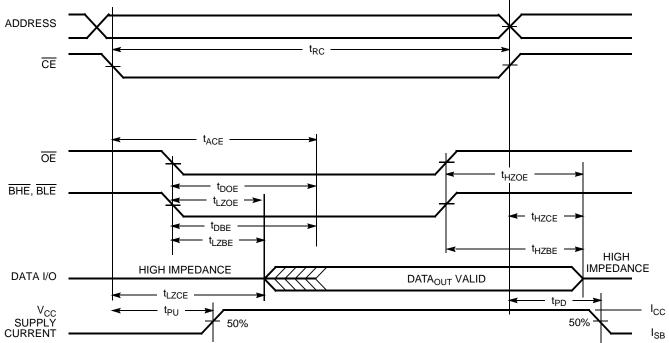
10. The minimum write cycle time for Write Cycle 2 (WE controlled, OE LOW) is the sum of tHZWE and tSD.



Switching Waveforms







Notes

- 11. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BHE} or both = V_{IL} , and $CE_2 = V_{IH}$. 12. WE is HIGH for read cycle.

- 13. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE₂ transition HIGH. 14. \overline{CE} refers to the internal logical combination of $\overline{CE_1}$ and $\overline{CE_2}$ such that when $\overline{CE_1}$ is LOW and $\overline{CE_2}$ is HIGH, \overline{CE} is LOW. For all other combinations, \overline{CE} is HIGH.



Switching Waveforms (continued)

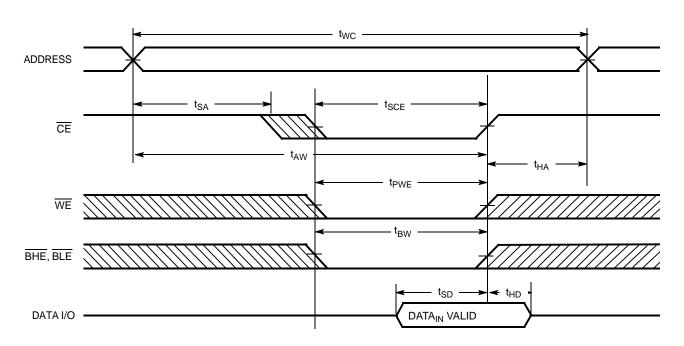
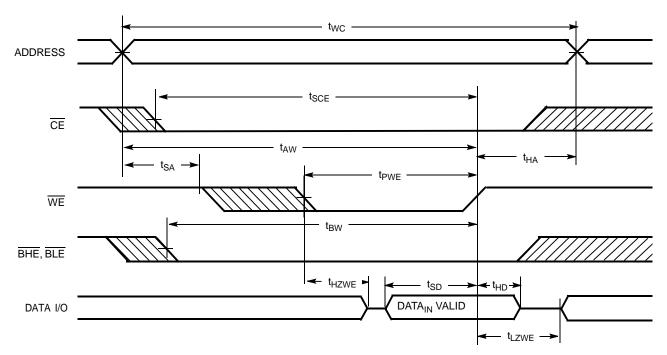


Figure 6. Write Cycle 1 (CE Controlled) ^[15, 16, 17]

Figure 7. Write Cycle 2 (WE Controlled, OE LOW) ^[15, 16, 17]



Notes

- 15. \overline{CE} refers to the internal logical combination of \overline{CE}_1 and CE_2 such that when \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW. For all other combinations, \overline{CE} is HIGH. 16. Data I/O is high impedance if \overline{OE} or B<u>HE</u>, BLE or both = V_{IH}. 17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.



Switching Waveforms (continued)

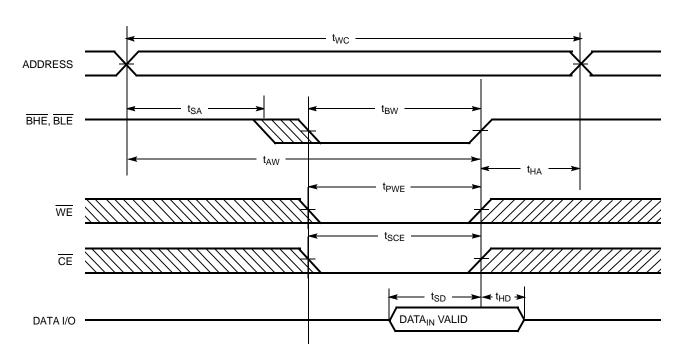


Figure 8. Write Cycle 3 (BLE or BHE Controlled) ^[18]

Truth Table

CE ₁	CE ₂	OE	WE	BLE	BHE	1/0 ₀ -1/0 ₇	I/O ₈ - I/O ₁₅	Mode	Power
Н	Х	Х	Х	Х	Х	High-Z	High-Z	Power down	Standby (I _{SB})
Х	L	Х	Х	Х	Х	High-Z	High-Z	Power down	Standby (I _{SB})
L	Н	L	Н	L	L	Data Out	Data Out	Read all bits	Active (I _{CC})
L	Н	L	Н	L	Н	Data Out	High-Z	Read lower bits only	Active (I _{CC})
L	Н	L	Н	Н	L	High-Z	Data Out	Read upper bits only	Active (I _{CC})
L	Н	Х	L	L	L	Data In	Data In	Write all bits	Active (I _{CC})
L	Н	Х	L	L	Н	Data In	High-Z	Write lower bits only	Active (I _{CC})
L	Н	Х	L	Н	L	High-Z	Data In	Write upper bits only	Active (I _{CC})
L	Н	Н	Н	Х	Х	High-Z	High-Z	Selected, Outputs disabled	Active (I _{CC})

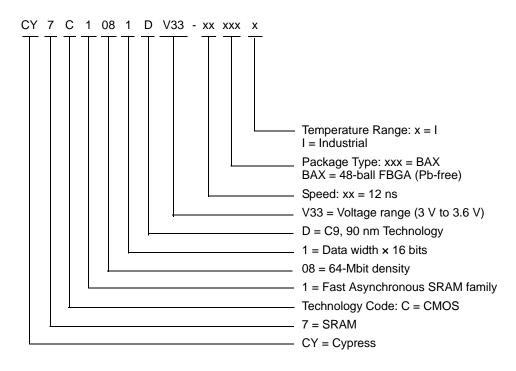
Note _______ 18. CE refers to the internal logical combination of \overline{CE}_1 and CE_2 such that when \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW. For all other combinations, \overline{CE} is HIGH.



Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1081DV33-12BAXI	001-50044	48-Ball FBGA (8 × 9.5 × 1.4 mm) (Pb-free)	Industrial

Ordering Code Definition





001-50044 *C

Package Diagram

Package : Body Size:

Ball Pitch : Total Thickness :

Mold Thickness :

Ball Diameter :

Mold Flatness :

Coplanarity:

Ball Count :

Stand Off : Ball Width :

Substrate Thickness :

Package Edge Tolerance :

Ball Offset (Package) :

Edge Ball Center to Center :

Ball Offset (Ball) :

•	, , , , , , , , , , , , , , , , , , ,	,
	TOP VIEW	BOTTOM VIEW
	PIN A1 CORNER	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$
Symbol Common Dimensions FBGA FBGA E 8,00 D 9,30 eD 0,75 A 1.45 +/- 0.05 M 0.910 Ref. S 0.21 Ref. 0.30 A1 0.16-0.26 b b 0.27-0.37 aa 0.150 bbb 0.200 ddd 0.080 ref 0.300 n 48 1 3,750 D1 5,250		
NCE M0-205		

Figure 9. 48-Ball FBGA (8 x 9.5 x 1.4 mm) (001-50044)

NOTES :

1. JEDEC REFERENCE MO-20

X

2. PACKAGE WEIGHT : 0.2409g

3. DIMENSIONS IN MILLIMETERS

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
FBGA	fine ball grid array
I/O	input/output
SRAM	static random access memory
TTL	transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μΑ	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt



Document History Page

Document Title: CY7C1081DV33, 64-Mbit (4 M × 16) Static RAM Document Number: 001-53992				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2746867	07/31/2009	VKN/AESA	New datasheet
*A	3100499	12/02/2010	PRAS	Updated Note 14. Changed datasheet status from Preliminary to Final. Updated Package Diagram and Sales, Solutions, and Legal Information. Added Acronyms, Document Conventions and Ordering Code Definition.
*В	3178249	21/02/2011	PRAS	Post to external web
*C	3246293	05/04/2011	PRAS	Modified Figure 44-B all FBGA pin configuration.
*D	3720094	08/22/2012	TAVA	Minor Text edits.

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