

General Description

The IDT5V925BI is a high-performance, low skew, low jitter phase-locked loop (PLL) clock driver. It provides precise phase and frequency alignment of its clock outputs to an externally applied clock input or internal crystal oscillator. The IDT5V925BI has been specially designed to interface with Gigabit Ethernet and Fast Ethernet applications by providing a 125MHz clock from 25MHz input. It can also be programmed to provide output frequencies ranging from 3.125MHz to 160MHz with input frequencies ranging from 3.125MHz to 80MHz.

The IDT5V925BI includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the chip accepts a 10-30MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω. The on-chip crystal oscillator includes the feedback resistor and crystal capacitors (nominal load capacitance is 18pF).

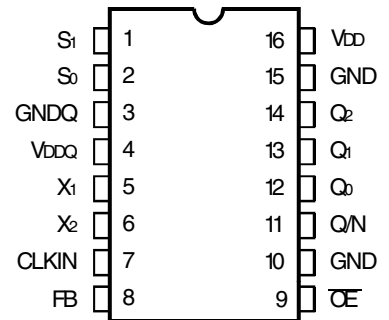
Applications

- Ethernet/fast ethernet
- Router
- Network switches
- SAN
- Instrumentation

Features

- 3V to 3.6V operating voltage
- 3.125MHz to 160MHz output frequency range
- Four programmable frequency LVCMOS/LVTTL outputs
- Input from fundamental crystal oscillator or external source
- Balanced drive outputs $\pm 12\text{mA}$
- PLL disable mode for low frequency testing
- Select inputs (S[1:0]) for divide selection (multiply ratio of 2, 3, 4, 5, 6, 7 and 8)
- 5V tolerant inputs
- Low output skew/jitter
- External PLL feedback, internal loop filter
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) package

Pin Assignment



IDT5V925BI

16 LEAD QSOP

0.194" x 0.236" x 0.058" package body

Q Package

Top View

Block Diagram

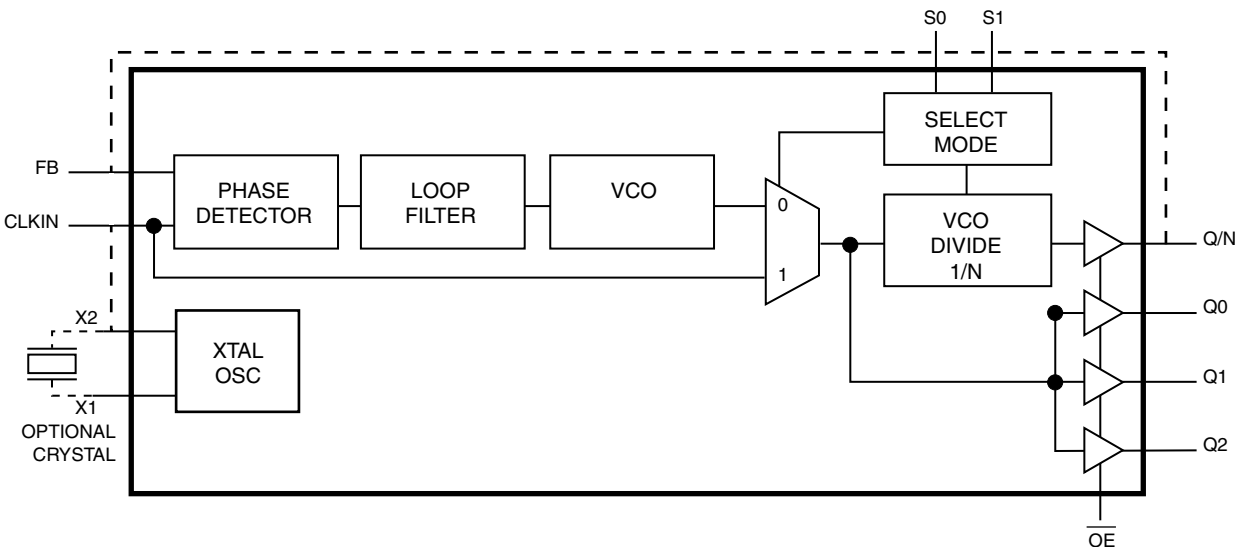


Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|------------|-------------------|--------|---------------------|---|
| 1, 2 | S1, S0 | Input | Pullup/ Pulldown | Three level divider/mode select pins. Float to MID. |
| 3 | GNDQ | Power | | Ground supply for PLL. |
| 4 | V _{DDQ} | Power | | Power supply for PLL. |
| 5 | X1 ⁽¹⁾ | Input | | Crystal oscillator input. Connected to GND if oscillator not required. |
| 6 | X2 ⁽¹⁾ | Output | | Crystal oscillator output. Leave unconnected for clock input. |
| 7 | CLKIN | Input | | Clock input. |
| 8 | FB | Input | | PLL feedback input which should be connected to Q/N output pin only. PLL locks onto positive edge of FB signal. |
| 9 | \overline{OE} | Input | | High-Impedance output enable. When asserted HIGH, clock outputs are high impedance. |
| 10, 15 | GND | Power | | Ground supply for output buffers. |
| 11 | Q/N | Output | | Programmable divide-by-N clock output. |
| 12, 13, 14 | Q0, Q1, Q2 | Output | | Output at N*CLKIN frequency. |
| 16 | V _{DD} | Power | | Power supply for output buffers. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

NOTE 1: For best accuracy, use parallel resonant crystal specified for a load capacitance of 18pF.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|--|-----------------------------------|---------|---------|---------|------------|
| C _{IN} | Input Capacitance | CLKIN, FB, \overline{OE} | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance (per output) | V _{DD} = 3.6V | | 15 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 47 | | k Ω |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 47 | | k Ω |
| R _{OUT} | Output Impedance | V _{DD} = 3.3V \pm 0.3V | | 16 | | Ω |

Function Tables

Table 3A. Function Table

| Output Used for Feedback | Allowable CLKIN Range (MHz) ^(1, 2) | | Output Frequency Relationships | |
|--------------------------|---|---------|--------------------------------|-----------|
| | Minimum | Maximum | Q/N | Q[2:0] |
| Q/N | 25/N | 160/N | CLKIN | CLKIN x N |

NOTE 1: Operation in the specified CLKIN frequency range guarantees that the VCO will operate in the optimal range of 25MHz to 160MHz. Operation with CLKIN outside specified frequency ranges may result in invalid or out-of-lock outputs.

NOTE 2: Q[2:0] are not allowed to be used as feedback.

Table 3B. Divide Selection Table ⁽¹⁾

| S1 | S0 | Divide-by-N Value | Mode |
|----|----|-----------------------------|---------------------|
| L | L | Factory Test ⁽²⁾ | |
| L | M | 2 | PLL |
| L | H | 3 | PLL |
| M | L | 4 | PLL |
| M | M | 5 ⁽³⁾ (default) | PLL |
| M | H | 6 | PLL |
| H | L | 7 | PLL |
| H | M | 8 | PLL |
| H | H | 16 | TEST ⁽⁴⁾ |

NOTE 1: H = HIGH, M = MEDIUM, L = LOW.

NOTE 2: Factory Test Mode: operation not specified.

NOTE 3: Ethernet mode (use a 25MHz input frequency and Q/N as feedback).

NOTE 4: Test mode for low frequency testing. In this mode, CLKIN bypasses the VCO (VCO powered down). Frequency must be > 1MHz due to dynamic circuits in the frequency dividers. Q[2:0] outputs are divided by 2 in test mode.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|-------------------------|
| Supply Voltage to Ground, V_{TERM} | -0.5V to +4.6V |
| DC Input Voltage, V_{IN} | -0.5V to +4.6V |
| DC Output Voltage, V_{OUT} | -0.5 to $V_{DD} + 0.5V$ |
| Maximum Power Dissipation, $T_A = 85^\circ C$ | 0.55W |
| Storage Temperature, T_{STG} | -65°C to +150°C |
| Package Thermal Impedance, θ_{JA} | 72.3°C/W |

Operating Conditions

| Symbol | Description | Minimum | Typical | Maximum | Units |
|--------------------|-----------------------|---------|---------|---------|-------|
| V_{DD} / V_{DDQ} | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| T_A | Operating Temperature | -40 | +25 | +85 | °C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 0.3V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------|---|---------|---------|---------|-------|
| I_{DDQ} | Quiescent Supply Current | $V_{DD} = V_{DDQ} = 3.6V$; CLKIN = 2.5MHz; S[1:0] = MM, $\overline{OE} = H$, All Outputs Unloaded | | 2 | 4 | mA |
| I_{DD} | Static Supply Current | $V_{DD} = V_{DDQ} = 3.6V$; S[1:0] = MM, $\overline{OE} = H$, All Outputs Unloaded | | 83 | 102 | mA |
| | Dynamic Supply Current | $V_{DD} = V_{DDQ} = 3.6V$, $f_{OUT} = 70MHz$; S[1:0] = LM, $\overline{OE} = GND$, All Outputs Loaded with 50Ω to GND | | 80 | 160 | mA |

NOTE: H = HIGH, M = MEDIUM, L = LOW

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 0.3V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|--------------------------|---|------------------|---------|------------------|---------|
| V_{IL} | Input Low Voltage | | | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2 | | | V |
| V_{IHH} | Input High Voltage | S[1:0] 3-Level Input Only | $V_{DD} - 0.6$ | | | V |
| V_{IMM} | Input Mid Voltage | S[1:0] 3-Level Input Only | $V_{DD}/2 - 0.3$ | | $V_{DD}/2 + 0.3$ | V |
| $V_{ILL}^{(1)}$ | Input Low Voltage | S[1:0] 3-Level Input Only | | | 0.6 | V |
| $I_{IN}^{(1)}$ | Input Leakage Current | CLKIN, FB $V_{IN} = V_{DD}$ or GND, $V_{DD} = \text{Max.}$ | -5 | | +5 | μA |
| $I_3^{(1)}$ | 3-Level Input DC Current | $V_{IN} = V_{DD}$, HIGH Level | | | 200 | μA |
| | | $V_{IN} = V_{DD}/2$, MID Level | -50 | | +50 | μA |
| | | $V_{IN} = \text{GND}$, LOW Level | -200 | | | μA |
| I_{IH} | Input High Current | $V_{IN} = V_{DD}$ | -5 | 0.07 | ± 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = 12\text{mA}$ | | 0.15 | 0.55 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -12\text{mA}$ | 2.4 | 2.8 | | V |

NOTE: Conditions apply unless otherwise specified.

NOTE 1: These inputs are normally wired to V_{DD} , GND, or unconnected. If the inputs are switched in real time, the function and timing of the outputs may glitch, and the PLL may require an additional lock time before all the datasheet limits are achieved.

Table 5. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 30 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = 3.3V \pm 0.3V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------|--|-----------------|---------|---------|---------|-------|
| t_R / t_F | Rise and Fall Time; NOTE 1 | 0.8V to 2V | | 0.7 | 1.8 | ns |
| odc | Output Duty Cycle; NOTE 1, 2 | | 44 | | 56 | % |
| t_{PD} | Propagation Delay; NOTE 1, 2 | CLKIN to FB | 50 | | 450 | ps |
| $t_{sk(o)}$ | Output-to-Output Skew; NOTE 1, 3, 4 | Q[2:0] | | | 110 | ps |
| | | Q/N - Q[2:0] | | | 450 | ps |
| $t_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 1, 3 | | | | 300 | ps |
| f_{OUT} | Output Frequency | | 25 | | 160 | MHz |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: JEDEC Standard 65.

NOTE 1: Guaranteed by design but not production tested.

NOTE 2: Measured from $V_{DD}/2$ of the input crossing point to the output at $V_{DD}/2$.

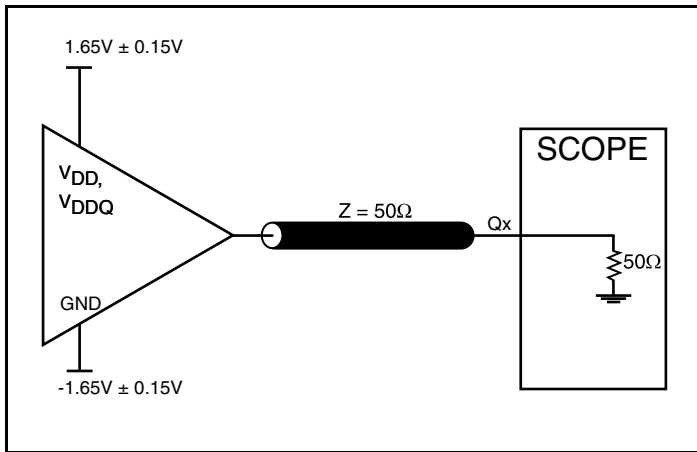
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.

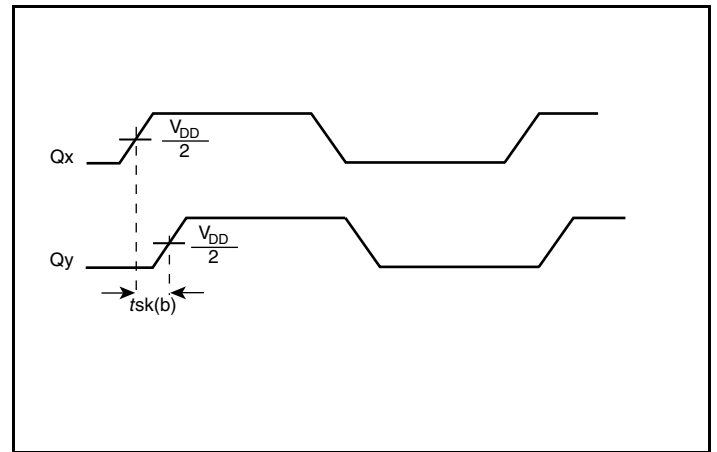
Table 6B. Input Timing Requirements, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Maximum | Units |
|-----------|------------------------------|-----------------|---------|---------|-------|
| f_{osc} | Crystal Oscillator Frequency | | 10 | 30 | MHz |
| f_{IN} | Input Frequency | | 25/N | 160/N | MHz |

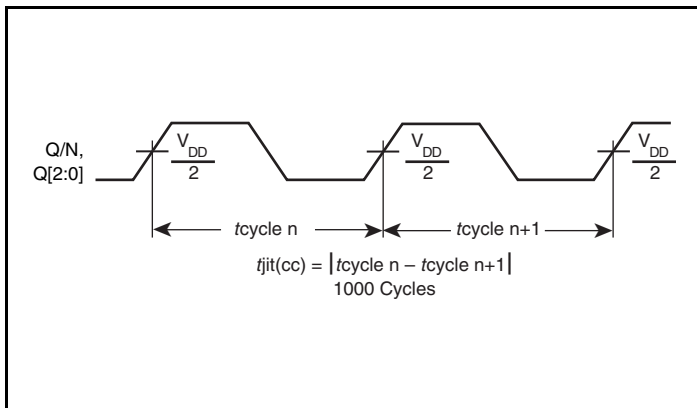
Parameter Measurement Information



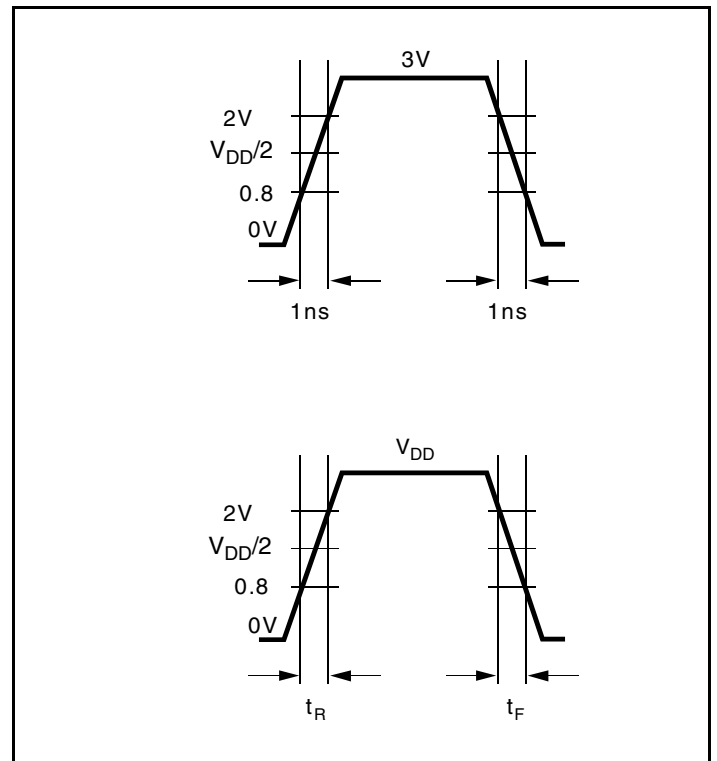
LVC MOS Output Load AC Test Circuit



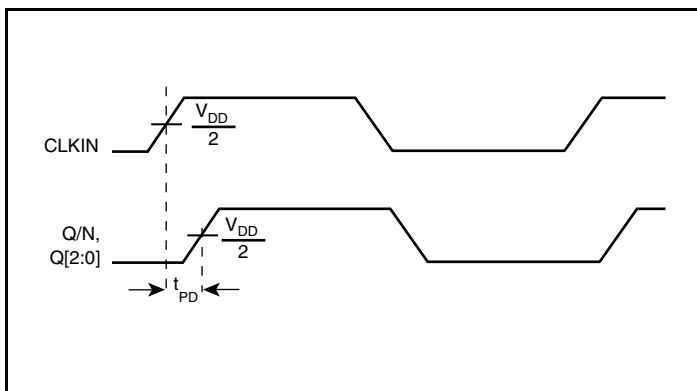
Output Skew



Cycle-to-Cycle Jitter

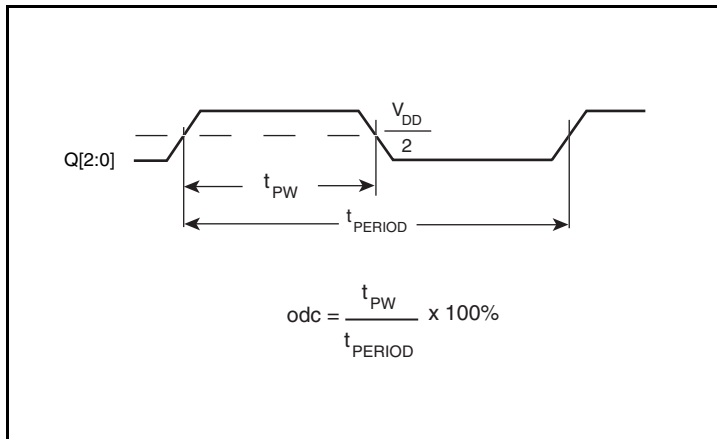


Input and Output Test Waveforms



Propagation Delay

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLKIN Input

For applications not requiring the use of a clock input, but using the crystal interface, the CLKIN input has to be connected to X2 (output of the crystal oscillator). See Figure 3.

Crystal Inputs

For applications not requiring the use of the crystal oscillator, X2 should be left floating and X1 and should be tied to ground. See Figure 2.

LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

How to Use the IDT5V925BI

The IDT5V925BI is a general-purpose phase-locked loop (PLL) that can be used as a zero delay buffer or a clock multiplier. It generates three outputs at the VCO frequency and one output at the VCO frequency divided by n, where n is determined by the Mode/Frequency Select input pins S0 and S1. The PLL will adjust the VCO frequency (within the limits of the Function Table) to ensure that the input frequency equals the Q/N frequency.

The IDT5V925BI can accept two types of input signals. The first is a reference clock generated by another device on the board which needs to be reproduced with a minimal delay between the incoming clock and output. The second is an external crystal. When used in the first mode, the crystal input (X1) should be tied to ground and the crystal output (X2) should be left unconnected.

By connecting Q/N to FB (see Figure 1), the IDT5V925BI not only becomes a zero delay buffer, but also a clock multiplier. With proper selection of S0 and S1, the Q0–Q2 outputs will generate two, three, or up to eight times the input clock frequency. Make sure that the input and output frequency specifications are not violated (refer to Function Table). There are some applications where higher fan-out is required. These kinds of applications could be addressed by using the IDT5V925BI in conjunction with a clock buffer such as the 49FCT3805. Figure 2 shows how higher fan-out with different clock rates can be generated.

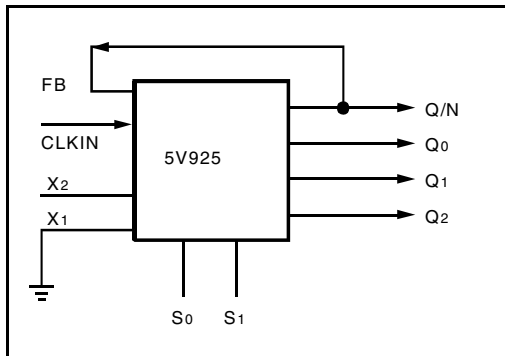


Figure 1

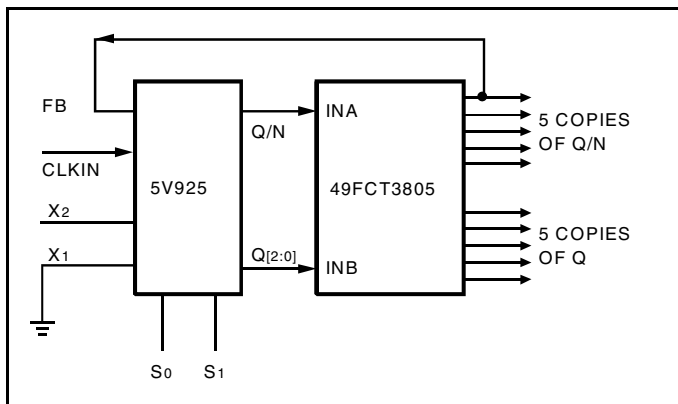


Figure 2

By connecting one of the 49FCT3505 outputs to the FB input of the IDT5V925BI, the propagation delay from CLKIN to the output of the 49FCT3505 will be nearly zero. To ensure PLL stability, only one 49FCT3505 should be included between Q/N and FB.

The second way to drive the input of the IDT5V925BI is via an external crystal. When connecting an external crystal to pins 5 and 6, the X2 pin must be shorted to the CLKIN (pin 7) as shown in Figure 3. To reduce the parasitic between the external crystal and the IDT5V925BI, it is recommended to connect the crystal as close as possible to the X1 and X2 pins.

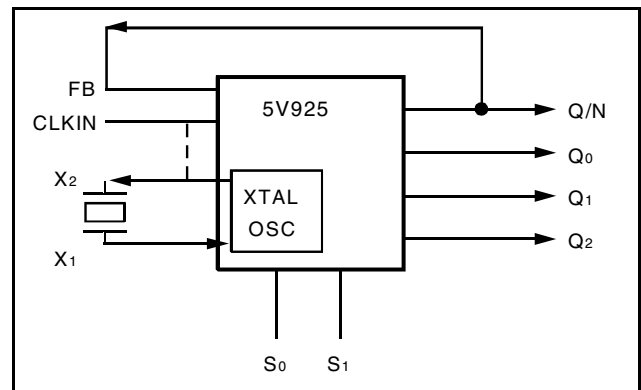


Figure 3

One of the questions often asked is what is the accuracy of our clock generators? In applications where clock synthesizers are used, the terms frequency accuracy and frequency error are used interchangeably. Here, frequency accuracy (or error) is based on two factors. One is the input frequency and the other is the multiplication factor. Clock multipliers (or synthesizers) are governed by the equation:

$$F_{OUT} = \frac{M}{N} \times F_{IN}$$

Where “M” is the feedback divide and “N” is the reference divide. If the ratio of M/N is not an integer, then the output frequency will not be an exact multiple of the input. On the other hand, if the ratio is a whole number, the output clock would be an exact multiple of the input. In the case of IDT5V925BI, since the reference divide (“N”) is “1”, the equation is a strong function of the feedback divide (“M”). In addition, since the feedback is an integer, the output frequency error (or accuracy) is merely a function of how accurate the input is. For instance, IDT5V925BI could accept two forms of input, one from a crystal oscillator (see Figure 1) and the other from a crystal (see Figure 3). By using a 20MHz clock with a multiplication factor of 5 (with an accuracy of ±30 parts per million), one can easily have three copies of 100MHz of clock with ±30ppm of accuracy. Frequency accuracy is defined by the following equation:

$$\text{Accuracy} = \frac{\text{Measured Frequency} - \text{Nominal Frequency} \times 10^6}{\text{Nominal Frequency}}$$

Where measured frequency is the average frequency over certain number of cycles (typically 10,000) and the nominal frequency is the desired frequency.

Schematic Examples

Figures 4A and 4B show an examples of IDT5V925BI application schematic. In Figure 4A example, the device is operated at $V_{DD} = V_{DDQ} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance, $C1 = 27pF$ and $C2 = 27pF$ are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting

$C1$ and $C2$. In Figure 4B example, the LVCMOS clock reference input is used.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT5V925BI provides separate power supplies to isolate from coupling into the internal PLL.

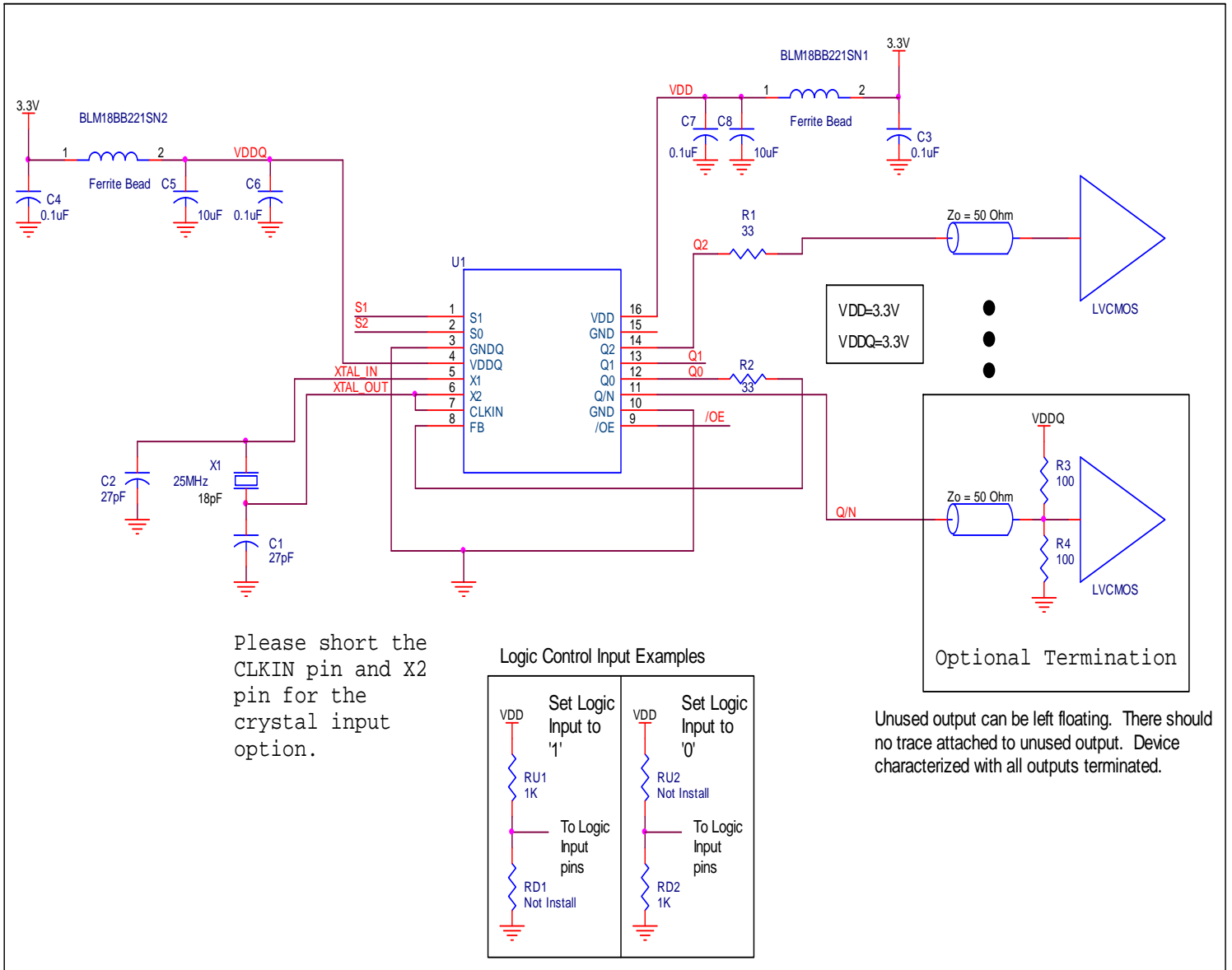


Figure 4A. IDT5V925BI Application Schematic with Crystal Input Reference

Schematic Examples, continued

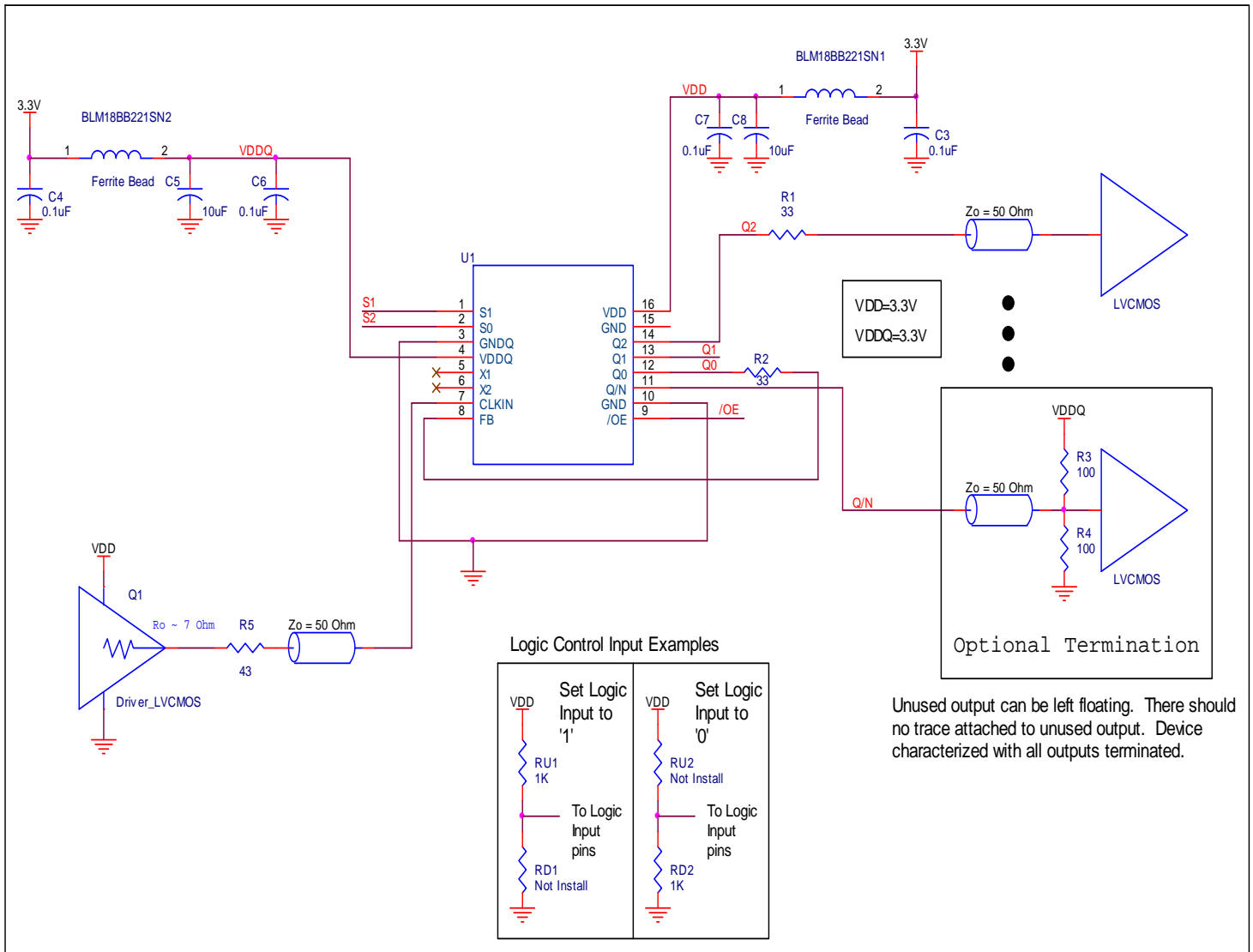


Figure 4B. IDT5V925BI Application Schematic with LVCMOS Reference Clock Input

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz.

If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT5V925BI. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT5V925BI is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 0.3V = 3.6V$, which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD_MAX(Static)} = 102mA$$

$$I_{DDQ_MAX} = 4mA$$

$$C_L = 5pF$$

N = number of outputs

$$C_{PD} = 15pF$$

Core Output Power Dissipation

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX(Static)} + I_{DDQ_MAX}) = 3.6V * (102mA + 4mA) = \mathbf{382mW}$

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
Output Current $I_{OUT} = V_{DD_MAX} / [2 * (50\Omega + R_{OUT})] = 3.6V / [2 * (50\Omega + 16\Omega)] = \mathbf{27.3mA}$
- Power Dissipation on the R_{OUT} per LVCMOS output
Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2 = 16\Omega * (27.3mA)^2 = \mathbf{11.9mW}$ per output
- Total Power Dissipation on the R_{OUT}
Total Power (R_{OUT}) = $11.9mW * 3 = \mathbf{35.7mW}$

Dynamic Power Dissipation

- Dynamic Power Dissipation at 160MHz
Total Power (160MHz) = $[(C_{PD} + C_L) * N] * Frequency * (V_{DD})^2 = [(15pF + 5pF) * 3] * 160MHz * (3.6V)^2 = \mathbf{124.4mW}$

Total Power Dissipation

- Total Power**
= Power (core) + Total Power (R_{OUT}) + Total Power (160MHz)
= $382mW + 35.7mW + 124.4mW$
= **542mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 72.3°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.542\text{W} * 72.3^\circ\text{C}/\text{W} = 124.2^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16-lead QSOP, Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 72.3°C/W | 64.4°C/W | 60.0°C/W |

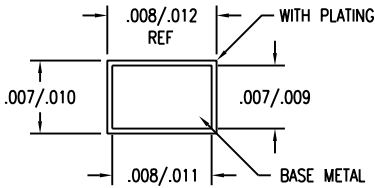
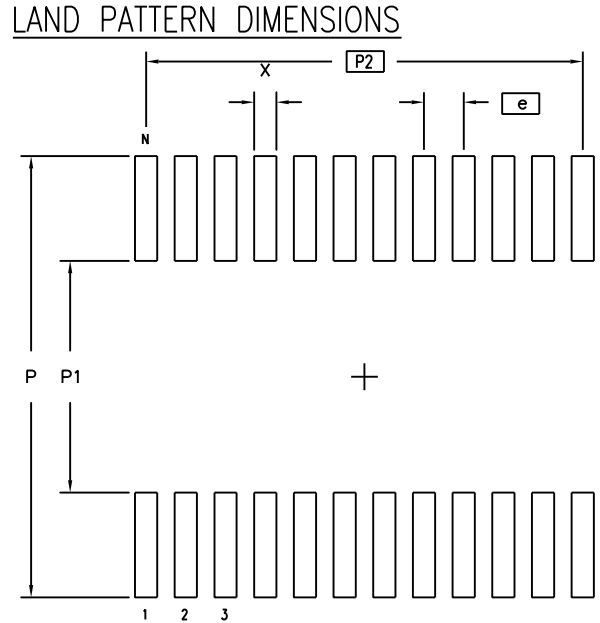
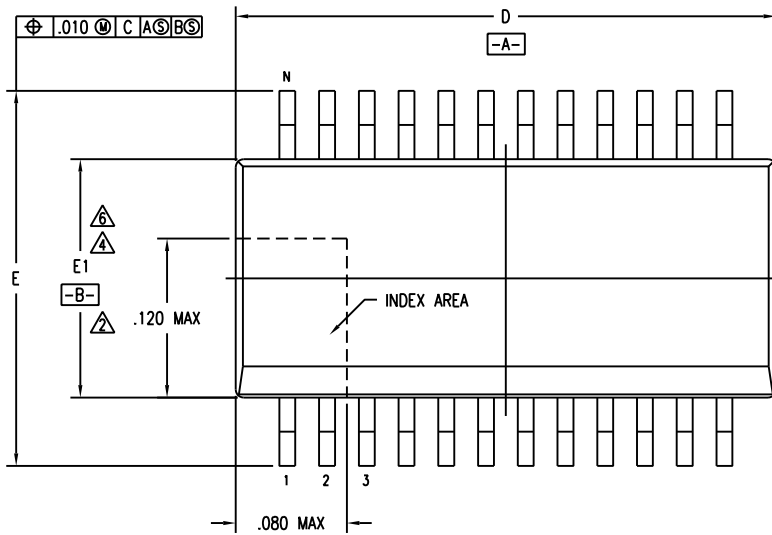
Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a Q Suffix, 16-lead QSOP

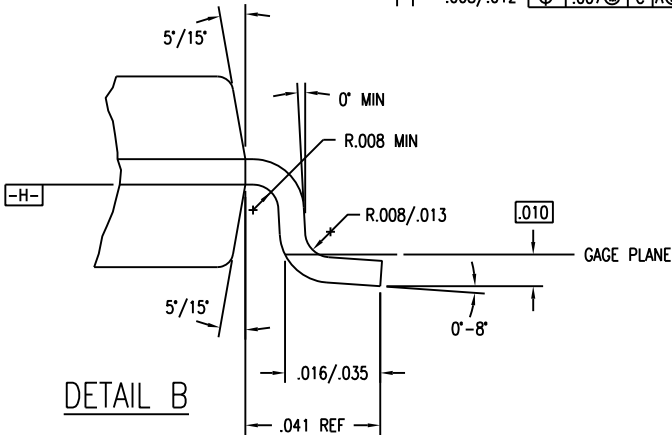
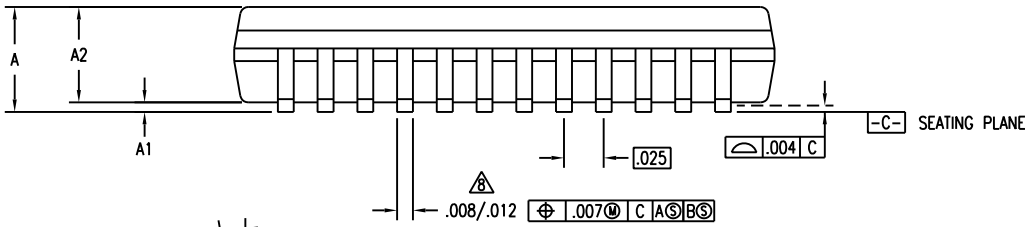
| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 72.3°C/W | 64.4°C/W | 60.0°C/W |

Package Outline and Package Dimensions

Package Outline - Q Suffix for 16 Lead QSOP



SECTION A-A



DETAIL B

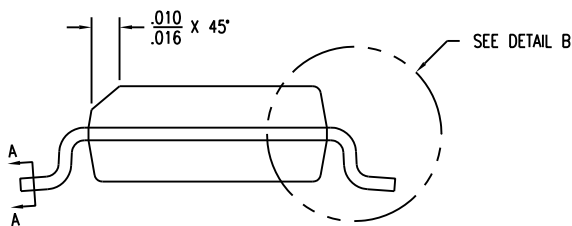


Table 9. Package Dimensions

| JEDEC Variation: AB | | | |
|--------------------------|-------------|---------|---------|
| All Dimensions in Inches | | | |
| Symbol | Minimum | Nominal | Maximum |
| N | 16 | | |
| A | 0.061 | 0.064 | .068 |
| A1 | 0.004 | 0.006 | 0.010 |
| A2 | 0.055 | 0.058 | 0.061 |
| D | 0.189 | 0.194 | 0.196 |
| E | 0.230 | 0.236 | 0.244 |
| E1 | 0.150 | 0.155 | 0.157 |
| P | 0.274 | | 0.282 |
| P1 | 0.142 | | 0.150 |
| P2 | 0.175 Basic | | |
| e | 0.025 Basic | | |
| x | 0.010 | | 0.018 |

Ref. Document: IDT PC/PCG Package Outline, Dwg# PSC-4040

Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|---------------|
| 5V925BQGI | IDT5V925BQGI | "Lead-Free" 16 Lead QSOP | Tube | -40°C to 85°C |
| 5V925BQGI8 | IDT5V925BQGI | "Lead-Free" 16 Lead QSOP | 3000 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|---------|---|----------|
| B | | 8 10 | Applications for Unused I/O Pins application note - corrected Input descriptions. Deleted Overdriving the XTAL Interface application note. | 1/21/11 |
| C | 10 | 16 | Removed leaded parts from ordering information table | 01/07/13 |

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