MOTOROLA

Switch Mode Power Supply with Multiple Linear Regulators and High Speed CAN Transceiver

33394

MULTI–OUTPUT POWER SUPPLY

SEMICONDUCTOR TECHNICAL DATA

The 33394 is a multi–output power supply integrated circuit with high speed CAN transceiver. The IC incorporates a switching pre–regulator operating over a wide input voltage range from +4.0V to +26.5V (with transients up to 45V).

The switching regulator has an internal 3.0A current limit and runs in both buck mode or boost mode to always supply a pre–regulated output followed by Low Drop Out (LDO) regulators: VDDH / 5.0V @ 400mA; VDD3_3 / 3.3V @ 120mA; VDDL / 2.6V (User scalable between 3.3V – 1.25V) @ 400mA typically, using an external NPN pass transistor. The Keep Alive regulator VKAM (scalable) @ 50mA; FLASH memory programming voltage VPP / 5.0V or 3.3V @ 150mA; three sensor supply outputs VREF(1,2,3) / 5.0V (tracking VDDH) @ 100mA each; and a switched battery output (VSEN) to supply 125mA clamped to 17V.

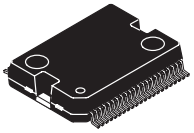
Additional features include Active Reset circuitry watching VDDH, VDD3_3, VDDL and VKAM, user selectable Hardware Reset Timer (HRT), Power Sequencing circuitry guarantees the core supply voltages never exceed their limits or polarities during system power up and power down.

A high speed CAN transceiver physical layer interfaces between the microcontroller CMOS outputs and differential bus lines. The CAN driver is short circuit protected and tolerant of loss of battery or ground conditions.

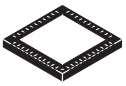
33394 is designed specifically to meet the needs of modules, which use the MPC565 microcontroller, though it will also support others from the MPC5XX family of Motorola microcontrollers.

Features:

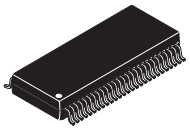
- Wide operating input voltage range: +4.0V to +26.5V (+45V transient).
- Provides all regulated voltages for MPC5XX MCUs and other ECU's logic and analog functions.
- Accurate power up/down sequencing.
- Provides necessary MCU support monitoring and fail–safe support.
- Provides three 5.0 V buffer supplies for internal & external (short–circuit protected) sensors.
- Includes step–down/step–up switching regulator to provide supply voltages during different battery conditions.
- Interfaces Directly to Standard 5.0V I/O for CMOS Microprocessors by means of Serial Peripheral Interface.



44–Lead HSOP
DH SUFFIX
CASE 1291

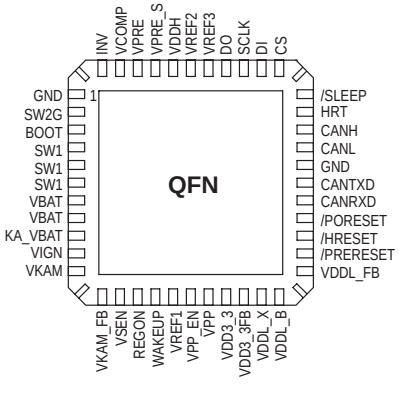


44–Lead QFN
FC SUFFIX
CASE 1310
(BOTTOM VIEW)

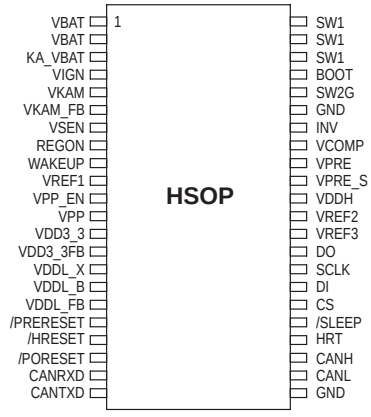


54–Lead SOICW–EP
DWB SUFFIX
CASE 1377

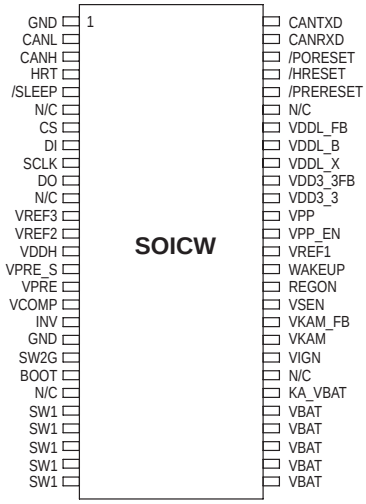
PIN CONNECTIONS



TOP VIEW



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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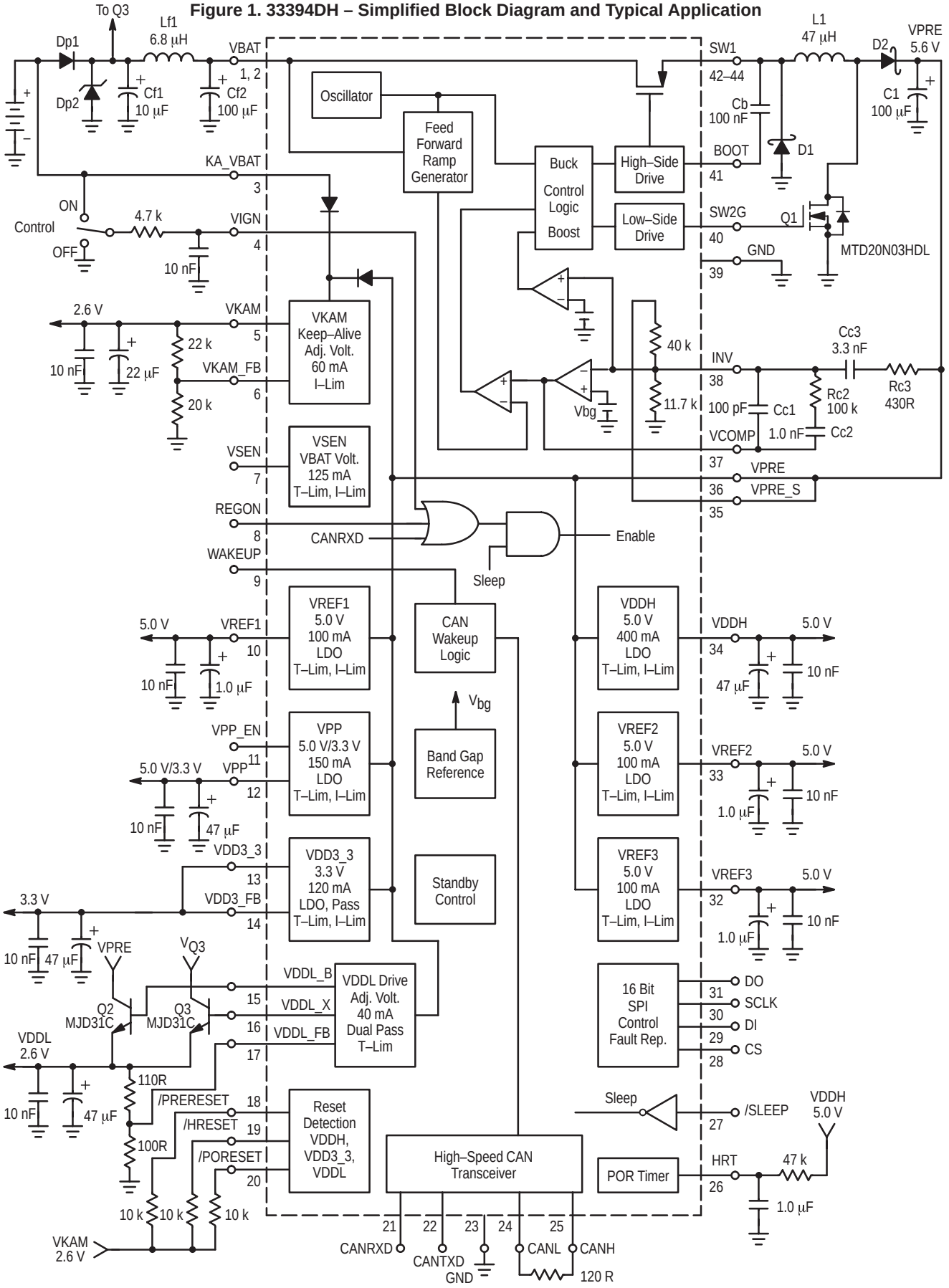
Figure 1. 33394DH – Simplified Block Diagram and Typical Application



Notes: 1. In this configuration the device can operate with a minimum input voltage VBAT of 4.0 V (voltage at 33394 VBAT pins).
2.VDDL and VKAM are adjustable to support current microprocessor technology (1.25 V to 3.3 V) by means of an external resistor divider.
3. When the 33394 CAN transceiver is not used, CANL and CANH pins can be shorted together.
4. Dp1 = reverse battery protection diode. Dp2 = load dump protection diode. Dp1, Dp2 can be ommitted in those applications which do not require such protection.

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PIN FUNCTION DESCRIPTION (44–HSOP Package)

PIN NO.	NAME	DESCRIPTION
1	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
2	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
3	KA_VBAT	Keep alive supply (with internal protection diode)
4	VIGN	Turn–On control through ignition switch (with internal protection diode)
5	VKAM	VDDL tracking Keep Alive Memory (Standby) supply
6	VKAM_FB	VKAM output feedback
7	VSEN	Switched battery output
8	REGON	Regulator “Hold On” input
9	WAKEUP	CAN wake up event output
10	VREF1	VDDH tracking linear regulator 1
11	VPP_EN	VPP enable
12	VPP	5.0 V/ 3.3 V FLASH memory programming supply, tracking VDDH/VDD3_3
13	VDD3_3	3.3 V regulated supply output, base drive for optional external pass transistor
14	VDD3_3FB	VDD3_3 output feedback
15	VDDL_X	VDDL optional external pass transistor base drive, operating in Boost Mode only
16	VDDL_B	VDDL external pass transistor base drive
17	VDDL_FB	VDDL output feedback
18	/PRERESET	Open drain /PRERESET output, occurs 0.7 us prior to /HRESET (Hardware Reset)
19	/HRESET	Open drain / HRESET (Hardware Reset) output
20	/PORESET	Open drain / PORESET (Power On Reset) supervising VKAM supply to the microprocessor.
21	CANRXD	CAN receive data (DOUT)
22	CANTXD	CAN transmit data (DIN)
23	GND	Ground
24	CANL	CAN differential bus drive low line
25	CANH	CAN differential bus drive high line
26	HRT	Hardware Reset Timer pin (programmed with external capacitor and resistor)
27	/SLEEP	Sleep Mode & Power Down control
28	CS	SPI chip select
29	DI	SPI serial data in
30	SCLK	SPI clock input
31	DO	SPI serial data out
32	VREF3	VDDH tracking linear regulator 3
33	VREF2	VDDH tracking linear regulator 2
34	VDDH	5.0 V regulated supply output
35	VPRE_S	Switching pre–regulator output sense
36	VPRE	Switching pre–regulator output
37	VCOMP	Switching pre–regulator compensation (error amplifier output)
38	INV	Switching pre–regulator error amplifier inverting input
39	GND	Ground
40	SW2G	External power switch (MOSFET) gate drive — Boost regulator
41	BOOT	Bootstrap capacitor
42	SW1	Source of the internal power switch (n–channel MOSFET)
43	SW1	Source of the internal power switch (n–channel MOSFET)
44	SW1	Source of the internal power switch (n–channel MOSFET)

NOTE: The exposed pad of the 44 HSOP package is electrically and thermally connected with the IC ground.

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PIN FUNCTION DESCRIPTION (44–QFN Package)

PIN NO.	NAME	DESCRIPTION
1	GND	Ground
2	SW2G	External power switch (MOSFET) gate drive — Boost Reg.
3	BOOT	Bootstrap capacitor
4	SW1	Source of the internal power switch (n–channel MOSFET)
5	SW1	Source of the internal power switch (n–channel MOSFET)
6	SW1	Source of the internal power switch (n–channel MOSFET)
7	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
8	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
9	KA_VBAT	Keep alive battery supply (with internal protection diode)
10	VIGN	Turn on control through ignition switch (with internal protection diode)
11	VKAM	VDDL tracking Keep Alive Memory (Standby) supply
12	VKAM_FB	VKAM output feedback
13	VSEN	Switched battery output
14	REGON	Regulator “Hold On” input
15	WAKEUP	CAN wake up event output
16	VREF1	VDDH tracking linear regulator 1
17	VPP_EN	VPP enable
18	VPP	5.0 V/ 3.3 V FLASH memory programming supply, tracking VDDH/VDD3_3
19	VDD3_3	3.3 V regulated supply output, base drive for optional external pass transistor
20	VDD3_3FB	VDD3_3 output feedback
21	VDDL_X	VDDL optional external pass transistor base drive, operating in Boost Mode only
22	VDDL_B	VDDL external pass transistor base drive
23	VDDL_FB	VDDL output feedback
24	/PRERESET	Open drain /PRERESET output, occurs 0.7 us prior to /HRESET (Hardware Reset)
25	/HRESET	Open drain / HRESET (Hardware Reset) output
26	/PORESET	Open drain / PORESET (Power On Reset) supervising VKAM supply to the microprocessor.
27	CANRXD	CAN receive data (DOUT)
28	CANTXD	CAN transmit data (DIN)
29	GND	Ground
30	CANL	CAN differential bus drive low line
31	CANH	CAN differential bus drive high line
32	HRT	Hardware Reset Timer pin (programmed with external capacitor and resistor)
33	/SLEEP	Sleep Mode & Power Down control
34	CS	SPI chip select
35	DI	SPI serial data in
36	SCLK	SPI clock input
37	DO	SPI serial data out
38	VREF3	VDDH tracking linear regulator 3
39	VREF2	VDDH tracking linear regulator 2
40	VDDH	5.0 V regulated supply output
41	VPRE_S	Switching pre–regulator output sense
42	VPRE	Switching pre–regulator output
43	VCOMP	Switching pre–regulator compensation (error amplifier output)
44	INV	Switching pre–regulator error amplifier inverting input

NOTE: The exposed pad of the 44 QFN package is electrically and thermally connected with the IC ground.

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PIN FUNCTION DESCRIPTION (54 SOICW–EP Package)

PIN NO.	NAME	DESCRIPTION
1	GND	Ground
2	CANL	CAN differential bus drive low line
3	CANH	CAN differential bus drive high line
4	HRT	Hardware Reset Timer pin (programmed with external capacitor and resistor)
5	/SLEEP	Sleep Mode & Power Down control
6	N/C	No Connect
7	CS	SPI chip select
8	DI	SPI serial data in
9	SCLK	SPI clock input
10	DO	SPI serial data out
11	N/C	No Connect
12	VREF3	VDDH tracking linear regulator 3
13	VREF2	VDDH tracking linear regulator 2
14	VDDH	5.0 V regulated supply output
15	VPRE_S	Switching pre–regulator output sense
16	VPRE	Switching pre–regulator output
17	VCOMP	Switching pre–regulator compensation (error amplifier output)
18	INV	Switching pre–regulator error amplifier inverting input
19	GND	Ground
20	SW2G	External power switch (MOSFET) gate drive — Boost regulator
21	BOOT	Bootstrap capacitor
23	SW1	Source of the internal power switch (n–channel MOSFET)
24	SW1	Source of the internal power switch (n–channel MOSFET)
25	SW1	Source of the internal power switch (n–channel MOSFET)
26	SW1	Source of the internal power switch (n–channel MOSFET)
27	SW1	Source of the internal power switch (n–channel MOSFET)
28	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
29	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
30	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
31	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
32	VBAT	Battery supply to IC (external reverse battery protection needed in some applications)
33	KA_VBAT	Keep alive supply (with internal protection diode)
34	N/C	No Connect
35	VIGN	Turn–On control through ignition switch (with internal protection diode)
36	VKAM	VDDL tracking Keep Alive Memory (Standby) supply
37	VKAM_FB	VKAM output feedback
38	VSEN	Switched battery output
39	REGON	Regulator “Hold On” input
40	WAKEUP	CAN wake up event output
41	VREF1	VDDH tracking linear regulator 1
42	VPP_EN	VPP enable
43	VPP	5.0 V/ 3.3 V FLASH memory programming supply, tracking VDDH/VDD3_3
44	VDD3_3	3.3 V regulated supply output, base drive for optional external pass transistor
45	VDD3_3FB	VDD3_3 output feedback
46	VDDL_X	VDDL optional external pass transistor base drive, operating in Boost Mode only
47	VDDL_B	VDDL external pass transistor base drive
48	VDDL_FB	VDDL output feedback
49	N/C	No Connect
50	/PRERESET	Open drain /PRERESET output, occurs 0.7 us prior to /HRESET (Hardware Reset)
51	/HRESET	Open drain / HRESET (Hardware Reset) output
52	/PORESET	Open drain / PORESET (Power On Reset) supervising VKAM supply to the microprocessor.
53	CANRXD	CAN receive data (DOUT)
54	CANTXD	CAN transmit data (DIN)

NOTE: The exposed pad of the 54 SOICW–EP package is electrically and thermally connected with the IC ground.

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1. MAXIMUM RATINGS (Maximum Ratings indicate sustained limits beyond which damage to the device may occur. Voltage parameters are absolute voltages referenced to ground.)

Parameter		Min.	Max.	Unit
Supply Voltage (VBAT), Load Dump		–0.3	+45	V
Supply Voltage (KA_VBAT, VIGN), Load Dump		–18	+45	V
Supply Voltages (VDDH, VPP, VDD3_3, VDDL, VKAM)		–0.3	+5.8	V
Supply Voltages (VREF1, VREF2, VREF3, VSEN)		–2.0	+18	V
CANL, CANH (0<VBAT<18 VDC no time limit)		–18	+26.5	V
ESD Voltage				
Human Body Model all pins	(Note 1)	–2.0	+2.0	kV
Machine Model all pins	(Note 2)	–200	+200	V
CANLesd, CANHesd	(Note 1)	–4.0	+4.0	kV
CANLesd, CANHesd	(Note 2)	–200	+200	V
CANLtransient, CANHtransient	(Note 3)	–200	+200	V
/SLEEP		–18	+45	V
REGON, VPP_EN, /HRESET, /PORESET, /PRERESET, HRT, DO, DI, CS, SCLK		–0.3	+7.0	V
CANTXD, CANRXD		–0.3	+7.0	V
Operational Package Temperature [Ambient Temperature]		–40	+125	°C
Storage Temperature		–65	+150	°C
Power Dissipation (T_A = 125°C)				
44 HSOP	(Note 4)		8.3	W
44 QFN	(Note 4)		5.0	W
54 SOICW–EP	(Note 4)		5.0	W
Lead Soldering Temperature	(Note 5)		260	°C
Maximum Junction Temperature			+150	°C
$R_{\theta JA}$, Thermal Resistance, Junction to Ambient (44 HSOP)	(Note 6)		41	°C/W
$R_{\theta JC}$, Thermal Resistance, Junction to Case (44 HSOP)	(Note 7)		0.2	°C/W
$R_{\theta JB}$, Thermal Resistance, Junction to Base (44 HSOP)	(Note 8)		3	°C/W
$R_{\theta JA}$, Thermal Resistance, Junction to Ambient (44 QFN)	(Note 6)		77	°C/W
$R_{\theta JC}$, Thermal Resistance, Junction to Case (44 QFN)	(Note 7)		1.7	°C/W
$R_{\theta JB}$, Thermal Resistance, Junction to Base (44 QFN)	(Note 8)		5.0	°C/W
$R_{\theta JA}$, Thermal Resistance, Junction to Ambient (54 SOICW–EP)	(Note 6)		52	°C/W
$R_{\theta JC}$, Thermal Resistance, Junction to Case (54 SOICW–EP)	(Note 7)		1.2	°C/W
$R_{\theta JB}$, Thermal Resistance, Junction to Base (54 SOICW–EP)	(Note 8)		8.1	°C/W

1. Human body model: C = 100 pF, R = 1.5 kΩ.
2. Machine model: C = 200 pF, R = 10 Ω and L = 0.75 µH. In case of a discharge from pin CANL to pin GND: – 100 V < CANL transient < +100 V; in case of a discharge from pin CANH to Vcc: –150 V < CANH transient < +150 V.
3. The waveforms of the applied transients is in accordance with ”ISO 7637 part 1” test pulses 1, 2, 3a and 3b.
4. Maximum power dissipation at indicated junction temperature.
5. Lead soldering temperature limit is for 10 seconds maximum duration; contact Motorola Sales Office for device immersion soldering time/temperature limits.
6. Thermal resistance measured in accordance with EIA/JESD51–2.
7. Theoretical thermal resistance from the die junction to the exposed pad.
8. Thermal resistance measured in accordance with JESD51–8.

2. RECOMMENDED OPERATING CONDITIONS (All voltages are with respect to ground unless otherwise noted)

Parameter		Value	Unit
Supply Voltages (VBAT, KA_VBAT)		4.0 to 26.5	V
Switching Regulator Output Current (I_{VPRE})	(Note 1)	0 to 1.2	A
VDDH Output Current		0 to 400	mA
VDD3_3 Output Current		0 to 120	mA
VDDL_B Pass Transistor Base Drive Current		0 to 40	mA
VPP Output Current		0 to 150	mA
VREF Output Current		0 to 100	mA
VSEN Output Current		0 to 125	mA
VKAM Standby Output Current (normal mode of operation)		0 to 60	mA
VKAM Standby Output Current (standby mode of operation)		0 to 12	mA

1. See Typical Application Diagram in Figure 1.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
GENERAL					
Start Up Voltage	$VBAT_{start}$			6.2	V
Power Dissipation, VBAT = 13.3 V (Buck Mode)			1.8		W
Undervoltage Shut Down	$VBAT_{UV}$	3.4		3.9	V
Battery Input Current, Power Down Mode, VIGN = 0 V; REGON = 0 V; I_{VKAM} = 0 mA, VBAT = 13.3 V; Battery Voltage = 14 V	$I_{VBAT(sleep)}$		750	1000	µA
Battery Input Current, Keep Alive Mode VIGN = 0; I_{VKAM} = –10 mA				12	mA
Power On Current, Regulator ON with no load on VDDH, VDD3_3, VDDL, VKAM, VREF, VPP, VSEN; VBAT = 13.3 V	$I_{VBAT(no\ load)}$			27	mA
Battery Input Current, VPRE = –1.0 A, VBAT = 4.5 V	$I_{VBAT(4.5)}$		2.2	3.0	A
Battery Input Current, VPRE = –1.0 A, VBAT = 9 V	$I_{VBAT(9)}$			1.5	A
Battery Input Current, VPRE = –1.0 A, VBAT = 13.3 V	$I_{VBAT(13.3)}$			1.2	A
Battery Input Current, VPRE = –1.0 A, VBAT = 18 V	$I_{VBAT(18)}$			1.1	A
MODE CONTROL					
VIGN Input Voltage Threshold, REGON = 0 V VBAT = 13.3 V; Battery Voltage = 14 V	V_{IH} V_{IL}	2.8 1.7	3.15 2.0	3.4 2.3	V
VIGN Hysteresis		0.7	1.0	1.5	V
VIGN Pull–Down Current, REGON = 0V VBAT = 13.3 V, Battery Voltage = 14 V, VIGN = 14 V	R_{PD}	40	100	150	µA
REGON Input High Voltage Threshold	V_{IH}	1.3	1.65	2.1	V
REGON Input Low Voltage Threshold	V_{IL}	0.8	1.35	1.5	V
REGON Input Voltage Threshold Hysteresis	V_{Ihys}	0.2	0.3	0.4	V
REGON Pull–Down Current, REGON = VDDH to $V_{IL(min)}$	R_{PD}	10	20	50	µA
/SLEEP Input High Voltage Threshold	V_{IH}	1.7	2.2	2.6	V
/SLEEP Input Low Voltage Threshold	V_{IL}	1.4	1.9	2.2	V
/SLEEP Input Voltage Threshold Hysteresis	V_{Ihys}	0.2	0.3	0.4	V
/SLEEP Pull–Down Current, /SLEEP = VDDH to $V_{IL(min)}$	R_{PD}	10	20	50	µA
VPP_EN Input High Voltage Threshold	V_{IH}	1.3	1.65	2.1	V
VPP_EN Input Voltage Low Threshold	V_{IL}	0.8	1.35	1.5	V
VPP_EN Pull–Down Current, VPP_EN = VDDH to $V_{IL(min)}$	R_{PD}	10	20	50	µA

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:						
BUCK CONVERTER						
Buck Converter Output Voltage, VBAT = 7.5V to 18V; I_{LOAD}=500mA		VPRE	5.4	5.6	5.8	V
Buck to Boost Mode Threshold Voltage	(Note 1)	$VBAT_{thd}$		6.7		V
Boost to Buck Mode Threshold Voltage	(Note 1)	$VBAT_{thu}$		7.2		V
N–channel power MOSFET SW1						
SW1 Drain–Source Breakdown Voltage	(Note 1)	BV_{DSS}	50			V
SW1 Continuous Drain Current		ID_{SW1}	–2.75			A
SW1 Drain–Source Current Limit		Isc_{SW1}	–2.5	–3.0	–3.5	A
SW1 Drain–Source On–Resistance; I_D = 1.0 A, VBAT = 9.0 V		$R_{DS(on)}$			300	mΩ
Error Amplifier (Design Information Only)						
Input Offset Voltage	(Note 1)	V_{OS}		20		mV
DC Open Loop Gain	(Note 1)	A_{VOL}		80		dB
Unity Gain Bandwidth	(Note 1)	BW		1.5		MHz
Output Voltage Swing — High Level	(Note 1)	V_{OH}		4.2		V
Output Voltage Swing — Low Level	(Note 1)	V_{OL}		0.4		V
Output Source Current	(Note 1)	I_{OUT}		1.0		mA
Output Sink Current	(Note 1)	I_{OUT}		200		µA
Ramp Generator						
Sawtooth Peak Voltage	(Note 1)	V_{OSC}			3.5	V
Sawtooth Peak–to–Peak Voltage	(Note 1)	$V_{OSCp–p}$			3.0	V
BOOST CONVERTER						
External Power MOSFET Gate Drive SW2G						
Boost Converter Output Voltage, VBAT = 4.5 V to 6.0 V	(Note 1)	VPRE	5.9	6.0	6.6	V
SW2G Output Voltage, Power MOSFET On	(Note 1)	V_g		VPRE		V
SW2G Source Continuous Current	(Note 1)	I_{source}		TBD		mA
SW2G Sink Continuous Current		I_{sink}	200	300	400	mA
AC CHARACTERISTICS:						
BUCK CONVERTER						
Oscillator Frequency		Freq	180	200	220	kHz
SW1 Switch Turn–ON Time	(Note 1)	$t_{T–ON}$		TBD		ns
SW1 Switch Turn–OFF Time	(Note 1)	$t_{T–OFF}$		TBD		ns
SW2G Switch Turn–ON Time, C_{gate} = pF	(Note 1)	$t_{T–ON}$		TBD		ns
SW2G Switch Turn–OFF Time, C_{gate} = pF	(Note 1)	$t_{T–OFF}$		TBD		ns
OFF Time	(Note 1)	t_{OFF}		1.25		µs
Duty cycle	(Note 1)	d		75		%

NOTE:
1. Guaranteed by design but not production tested.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
VDDH					
VDDH Output Voltage, I_{VDDH} = –400 mA;	VDDH	4.9	5.0	5.1	V
VDDH Load Regulation, VBAT = 13.3 V; I_{VDDH} = 0 to –400 mA;	$LoadRg_{VDDH}$	–40		40	mV
VDDH Line Regulation, VBAT = 4.0 V to 26.5 V; I_{VDDH} = –400 mA;	$LineRg_{VDDH}$	–20		20	mV
VDDH Drop Out Voltage, VPRE – VDDH, I_{VDDH} = –400 mA; Decrease VBAT until Resets asserted	V_{DOV}			450	mV
VDDH Output Current, VBAT = 4.0 V to 26.5 V	I_{VDDH}		–400		mA
VDDH Short Circuit Current, VDDH = 0 V	I_{SC}	–750		–440	mA
VDDH Maximum Allowed Feedback Current (Note 1) (Power Up Sequence Guaranteed) (Note 2)				135	µA
VDDH Reset Voltage, Range of VDDH where Resets must remain asserted	V_{VDDH_HRST}	0.5		4.8	V
Thermal Shutdown Junction Temperature (Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis (Note 1)	TS_{HYS}	5.0		20	°C
VDD3_3					
VDD3_3 Output Voltage, I_{VDD3_3} = –120 mA;	VDD3_3	3.21	3.3	3.36	V
VDD3_3 Load Regulation, VBAT = 13.3 V; I_{VDD3_3} = 0 to –120 mA	$LoadRg_{VDD3}$	–40		40	mV
VDD3_3 Line Regulation, VBAT = 4.0V to 26.5V; I_{VDD3_3} = –120mA	$LineRg_{VDD3}$	–20		20	mV
VDD3_3 Drop Out Voltage, VPRE – VDD3_3 I_{VDD3_3} = –120 mA; Decrease VBAT until Resets asserted	V_{DOV}			2.04	V
VDD3_3 Output Current, VBAT = 4.0 V to 26.5 V	I_{VDD3_3}		–120		mA
VDD3_3 Short Circuit Current, VDD3_3 = 0 V	I_{SC}	–320		–130	mA
VDD3_3 Maximum Allowed Feedback Current (Note 1) (Power Up Sequence Guaranteed) (Note 2)				135	µA
VDD3_3 Reset Voltage Range of VDD3_3 where Resets must remain asserted	V_{VDD3_HRST}	0.5		3.1	V
Thermal Shutdown Junction Temperature (Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis (Note 1)	TS_{HYS}	5.0		20	°C
VDDL					
VDDL Feedback Reference Voltage, pin VDDL_FB I_{VDDL_B} = 0 to –40 mA	$VDDL_{REF}$	1.242	1.267	1.292	V
VDDL Load Regulation, VBAT = 13.3 V; I_{VDDL_B} = 0 to –40 mA	$LoadRg_{VDDL}$	–1.6		0	%
VDDL Line Regulation VBAT = 4.0 V to 26.5 V; I_{VDDL_B} = –40 mA	$LineRg_{VDDL}$	–0.8		0.8	%
VDDL Drop Out Voltage, VPRE – VDDL I_{VDDL} = –400 mA; VBAT decreases until Resets asserted	V_{DOV}			1.3	V
VDDL Reset Voltage, (Note 1) Range of VDDL where Resets must remain asserted	V_{VDDL_HRST}	0.5		VDDL –5%	V
VDDL Susceptibility to Feeding Back (Note 3) (Power Up Sequence Guaranteed)	$VDDL_{REF}$			0.187	V
VDDL_B Drive Output Current, VBAT = 7.5V to 26.5V	I_{VDDL_B}		–40		mA
VDDL_B Drive Short Circuit Current VDDL_B = 0V, VBAT = 7.5V to 26.5V	Isc_{VDDL_B}	–100		–45	mA
VDDL_X Drive Output Current, VBAT = 4.0 V to 6 V	I_{VDDL_B}		–40		mA
VDDL_X Drive Short Circuit Current, VDDL_X = 0V, VBAT = 4.0V to 6V	Isc_{VDDL_X}	–100		–45	mA
VDDL Feedback VDDL_FB Input Current, VDDL_FB = 5.0 V	I_{VDDL_FB}	0		2.0	µA

NOTE:
1. Guaranteed by design but not production tested.
2. Maximum allowed current flowing back into the regulator output.
3. Voltage fed back into the VDDL output, which still guaranties proper Power Up sequencing.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
VKAM					
VKAM Feedback Reference Voltage, pin VKAM_FB Normal Mode (switcher running), I_{VKAM} = 0 to –50mA	$VKAM_{REF}$	1.242	1.267	1.292	V
VKAM Load Regulation, VBAT = 13.3 V; I_{VKAM} = –0 to –50 mA	$LoadRg_{VKAM}$	–1.6		0	%
VKAM Line Regulation, VBAT = 4.0 V to 26.5 V; I_{VKAM} = –50 mA	$LineRg_{VKAM}$	–0.8		0.8	%
VKAM Tracking to VDDL Voltage, VDDL – VKAM VBAT = 4.0 V to 26.5 V; I_{VKAM} = 0 to –50 mA, I_{VDDL} = 0 to –400mA	VT_{VKAM}	–1.6		0.8	%
VKAM Feedback Voltage — Power Down Mode 3.0 V ≤ Battery Voltage ≤ 26.5 V, I_{VKAM} = –12 mA	VKAM	0.675			V
VKAM Reset Voltage (/PORESET) Range of VKAM where Resets must remain asserted	V_{VKAM_HRST}	0.5		VKAM –5%	V
VKAM Output Current (Normal Mode), VBAT = 4.0 V to 26.5 V	I_{VKAM}		–50		mA
VKAM Output Current (Sleep Mode and when VBAT ≤ 4.0 V)	$I_{VKAM(sleep)}$		–12		mA
VKAM Short Circuit Current, VKAM = 0 V	I_{SC}	–140		–50	mA
VKAM Feedback VKAM_FB Input Current, VKAM_FB = 5.0 V	I_{VKAM_FB}	0		2.0	µA
VKAM Output Capacitance Required, Capacitor Initial Tolerance 10%		22		100	µF
VPP					
VPP 5.0V Output Voltage (Default), I_{VPP} = –150 mA	VPP_5	4.86	5.0	5.12	V
VPP 3.3 V Output Voltage (Programmed by SPI) I_{VPP} = –150 mA	VPP_3	3.22	3.3	3.38	V
VPP Load Regulation, VBAT = 13.3 V; I_{VPP} = 0 to –150 mA	$LoadRg_{VPP}$	–0.8		0.8	%
VPP Line Regulation, VBAT = 4.0 V to 26.5 V; I_{VPP} = –150 mA	$LineRg_{VPP}$	–0.4		0.4	%
VPP Tracking to VDDH Voltage, VDDH – VPP, VBAT = 4.0 V to 26.5 V; I_{VPP} = 0 to –150 mA; I_{VDDH} = 0 to –400 mA	VT_{VPP}	–0.8		0.8	%
VPP Drop Out Voltage, VPRE — VPP (VPP set to default 5.0V) I_{VPP} = –150 mA; Decrease VBAT until VPP is out of specification (less than 4.86 V)	V_{DOV}			0.4	V
VPP Output Current, VBAT = 4.0 V to 26.5 V	I_{VPP}		–150		mA
VPP Short Circuit Current, VPP = 0 V	I_{SC}	–360		–165	mA
Thermal Shutdown Junction Temperature (Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis (Note 1)	TS_{HYS}	5.0		20	°C

NOTE:
1. Guaranteed by design but not production tested.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
VREF1, 2, 3					
VREF Output Voltage, I_{VREF} = –100 mA	VREF	4.86	5.0	5.12	V
VREF Load Regulation, VBAT = 13.3 V; I_{VREF} = 0 to –100 mA	$LoadRg_{VREF}$	–40		40	mV
VREF Line Regulation, VBAT = 4.0 V to 26.5 V; I_{VREF} = –100 mA	$LineRg_{VREF}$	–20		20	mV
VREF Tracking to VDDH Voltage, VDDH – VREF, VBAT = 4.0 V to 26.5 V, I_{VREF} = 0 to –100 mA; I_{VDDH} = 0 to –400 mA	VT_{VREF}	–40		20	mV
VREF Drop Out Voltage, VPRE–VREF I_{VREF} = –100 mA; Decrease VBAT until VREF is out of specification (less than 4.86 V)	V_{DOV}			0.4	V
VREF Output Current, VBAT = 4.0 V to 26.5 V	I_{VREF}		–100		mA
VREF Short Circuit Current, VREF = –2.0 V	I_{SC}	–260		–110	mA
VREF Short to Battery Load Current, VBAT = 18 V, VREF = 18 V	$Istb_{VREF}$			40	mA
VREF Leakage Current, VREF disabled, VREF = –2.0 V	I_{LKVREF}	–2.0			mA
Thermal Shutdown Junction Temperature (Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis (Note 1)	TS_{HYS}	5.0		20	°C
VSEN					
VSEN Saturation Voltage, I_{VSEN} = 0 to –125 mA, VBAT= 8 to 16 V	$VSEN_{sat}$			0.2	V
VSEN Output Voltage Limit, I_{VSEN} = 0 to –125mA, VBAT= 16 to 26.5V	$VSEN_{limit}$	16	17	21	V
VSEN Short Circuit Current, VSEN = –2.0 V	Isc_{VSEN}	–290		–140	mA
VSEN Short to Battery Load Current, VBAT = 18 V, VSEN = 18 V	$Istb_{VSEN}$			40	mA
VSEN Leakage Current, VSEN disabled, VSEN = –2.0 V	I_{LKVSEN}			200	µA
Thermal Shutdown Junction Temperature (Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis (Note 1)	TS_{HYS}	5.0		20	°C

NOTE:
1. Guaranteed by design but not production tested.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
SUPERVISORY OUTPUTS					
Reset Voltage Thresholds /HRESET to follow /PRERESET by 0.7 µs					
VDDH Reset Upper Threshold Voltage (Note 1)				5.2	V
VDDH Reset Lower Threshold Voltage (Note 1)		4.8			V
VDD3_3 Reset Upper Threshold Voltage (Note 1)				3.43	V
VDD3_3 Reset Lower Threshold Voltage (Note 1)		3.17			V
VDDL Reset Upper Threshold Voltage (Notes 1, 4)				1.35	V
VDDL Reset Lower Threshold Voltage (Notes 1, 4)		1.2			V
/PORESET Voltage Threshold					
VKAM Reset Upper Threshold Voltage (Notes 2, 5)				1.35	V
VKAM Reset Lower Threshold Voltage (Notes 2, 5)		1.2			V
/PRERESET, /HRESET, /PORESET Open Drain Maximum Voltage (Note 3)				7.0	V
/PRERESET, /HRESET, /PORESET Open Drain Pull–Down Current, V_{reset}< 0.4 V				1.0	mA
/PRERESET, /HRESET, /PORESET Low–Level Output Voltage, IOL = 1.0 mA				0.5	V
/PRERESET /HRESET /PORESET Leakage Current				15	µA
WAKEUP High–Level Output Voltage, IOH = –800µA		VDDH–0.8			V
WAKEUP Low–Level Output Voltage, IOL = 1.6 mA				0.4	V
HRT Voltage Threshold		2.49	2.53	2.57	V
HRT Sink Current				1.0	mA
HRT Leakage Current				5.0	µA
HRT Saturation Voltage, HRT Current = 1 mA				0.4	V
AC CHARACTERISTICS:					
SUPERVISORY OUTPUTS					
/PORESET Delay Delay time from VKAM in regulation and stable to the release of /PORESET		7.0	10	15	ms
Reset Delay Time Time from fault on VDDH, VDD3_3, VDDL or VKAM to Reset (/PORESET, /PRERESET)		10	20	50	µs
/HRESET Delay Time Time From /PRERESET low to /HRESET low		0.5	0.7	1.0	µs
VDDH, VDDL, VREF Power Up Sequence Max Power Up Sequence Time Dependent on Output Load Characteristics. (Note 3)		800			µs

NOTE:
1. VDDH, VDD3_3, VDDL regulator outputs supervised by /PRERESET and /HRESET.
2. VKAM regulator output supervised by /PORESET.
3. Guaranteed by design but not production tested.
4. Measured at the VDDL_FB pin.
5. Measured at the VKAM_FB pin.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
CAN Transceiver (Bus Load CANH to CANL R_L = 60 Ω; Vdiff = $V_{CANH} – V_{CANL}$)					
CAN Transceiver Supply Current (dominant), V_{CANTXD} = 0V	$I_{DD(CAN)}$	30	50	70	mA
CAN Transceiver Supply Current (recessive), V_{CANTXD} = VDDH	$I_{DD(CAN)}$	2.5	5	10	mA
Transmitter Data Input CANTXD					
High–Level Input Voltage Threshold (recessive), Vdiff<0.5V	V_{IH}	1.4		2.0	V
Low–Level Input Voltage Threshold (dominant), Vdiff>1.0V	V_{IL}	0.8		1.4	V
High–Level Input Current, VCANTXD = VDDH	I_{IH}	–5	0	+5	µA
Low–Level Input Current, V_{CANTXD} = 0V	I_{IL}	–10	–15	–30	µA
CANTXD Pull–up Current, V_{CANTXD} = 0V to $V_{IH(max)}$	I_{PU}	–10		–60	µA
CANTXD Input Capacitance (Note 1)	$C_{I(TXD)}$		5	10	pF
Receiver Data Output CANRXD					
High–Level Output Voltage V_{CANTXD} = VDDH, I_{CANRXD} = –0.8 mA	V_{OH}	VDDH –0.8		VDDH	V
Low–Level Output Voltage, V_{CANTXD} = 0, I_{CANRXD} = 1.6 mA	V_{OL}			0.4	V
High–Level Output Current, V_{CANRXD} = 0.7VDDH	I_{OH}			–800	µA
Low–Level Output Current, V_{CANRXD} = 0.4V	I_{OL}			1.6	mA
BUS Lines CANH, CANL					
Output Voltage CANH (recessive) V_{CANTXD} = VDDH; R_L = open	$V_{CANH(r)}$	2.0	2.5	3.0	V
Output Voltage CANL (recessive) V_{CANTXD} = VDDH; R_L = open	$V_{CANL(r)}$	2.0	2.5	3.0	V
Output Current CANH (recessive) V_{CANTXD} = VDDH; V_{CANH}, V_{CANL} = 2.5V	$I_{O(CANH)(r)}$			100	µA
Output Current CANL (recessive) V_{CANTXD} = VDDH; V_{CANH}, V_{CANL} = 2.5V	$I_{O(CANL)(r)}$	–100			µA
Output Voltage CANH (dominant), V_{CANTXD} = 0V	$V_{CANH(d)}$	2.75	3.5	4.5	V
Output Voltage CANL (dominant), V_{CANTXD} = 0V	$V_{CANL(d)}$	0.5	1.5	2.25	V
Differential Output Voltage (dominant) $V_{CANH(d)} – V_{CANL(d)}$ V_{CANTXD} = 0V	$V_{Odiff(d)}$	1.5	2.0	3.0	V
Differential Output Voltage (recessive) $V_{CANH(r)} – V_{CANL(r)}$ V_{CANTXD} = VDDH	$V_{Odiff(r)}$	0		0.5	V
Differential Input Common Mode Voltage Range	V_{CM}	–2.0		7.0	V
Differential Receiver Threshold Voltage (recessive) V_{CANTXD} = VDDH, V_{CANRXD} < 0.4V, – 2.0V < V_{CM} < 7.0V	$V_{RXDdiff(th)}$	0.5	0.75	1.0	V
Differential Receiver Input Voltage Hysteresis	$V_{Idiff(hys)}$	0.10	0.2	0.30	V
Short Circuit Output Current CANH V_{CANH} = – 8.0V, V_{CANTXD} = 0V	$I_{SC(CANH)}$	–70		–200	mA
Short Circuit Output Current CANL V_{CANL} = VBAT = 18V, V_{CANTXD} = 0V	$I_{SC(CANL)}$	70		200	mA
Loss of Ground — see Figure 11. Refer to Figure 10 for loading considerations.					
Output Leakage Current CANH, V_{CANH} = –18V	$I_{OLKG(CANH)}$	–2.0		2.0	mA
Output Leakage Current CANHL, V_{CANL} = –18V	$I_{OLKG(CANL)}$	–2.0		2.0	mA
Loss of Battery — see Figure 12. Refer to Figure 10 for loading considerations.					
Input Leakage Current CANH, V_{CANH} = 6.0V	$I_{ILKG(CANH)}$	–800		800	µA
Input Leakage Current CANHL, V_{CANL} = 6.0V	$I_{ILKG(CANL)}$	–800		800	µA

NOTE:
1. Guaranteed by design but not production tested.

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:						
CAN Transceiver (Continued) (Bus Load CANH to CANL R_L = 60 Ω; Vdiff = $V_{CANH} – V_{CANL}$)						
CANH,CANL impedance						
CANH Common Mode Input Resistance		$R_{i(CM)CANH}$	5.0	25	50	kΩ
CANL Common Mode Input Resistance		$R_{i(CM)CANL}$	5.0	25	50	kΩ
CANH, CANL Common Mode Input Resistance Mismatch $100(R_{iCANH} – R_{i(CM)CANL})/[(R_{iCANH} + R_{i(CM)CANL})/2]$		$R_{i(CM)MCAN}$	–3.0		3.0	%
Differential Input Resistance		$R_{I(dif)}$	25	50	75	kΩ
CANH Input Capacitance, V_{CANTXD} = VDDH	(Note 1)	$C_{I(CANH)}$		7.5	20	pF
CANL Input Capacitance, V_{CANTXD} = VDDH	(Note 1)	$C_{I(CANL)}$		7.5	20	pF
Differential Input Capacitance, $C_{INCANH} – C_{INCANL}$, V_{CANTXD} = VDDH	(Note 1)	$C_{I(CANdif)}$		3.75	10	pF
Thermal Shutdown						
Thermal Shutdown Junction Temperature	(Note 1)	TS_{DIS}	150		190	°C
Thermal Shutdown Hysteresis	(Note 1)	TS_{HYS}	5.0		20	°C
AC CHARACTERISTICS:						
CAN Transceiver						
Timing Characteristics						
See Figure 2, CANTXD = 250 kHz square wave; CANH & CANL Load R_L = 60 Ω differential.						
Delay CANTXD to Bus Active, C_L = 3nF		t_{onTXD}			50	ns
Delay CANTXD to Bus Inactive, C_L = 10pF		t_{offTXD}			80	ns
Delay CANTXD to CANRXD, Bus Active, C_L = 3nF		t_{onRXD}			120	ns
Delay CANTXD to CANRXD, Bus Inactive, C_L = 10pF		t_{offRXD}			190	ns

NOTE:
1. Guaranteed by design but not production tested.

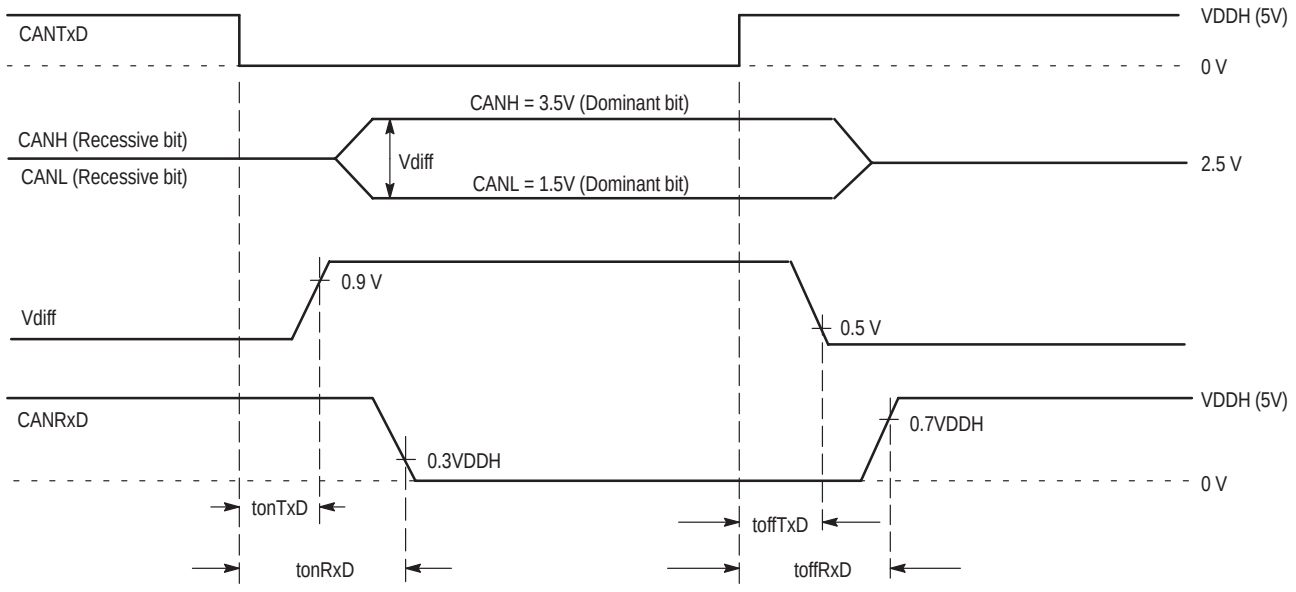

Figure 2. CAN Delay Timing Waveform

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3. ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C; +4.0 V ≤ VBAT ≤ +26.5 V using the 33394 typical application circuit – see Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS:					
SPI					
DO Output High Voltage, I_{OH} = –100 µA	V_{OH}	4.2			V
DO Output Low Voltage, I_{OL} = 1.6 mA	V_{OL}			0.4	V
DO Tri–state Leakage Current, CS = 0	I_{DOLkg}	–10		10	µA
CS, SCLK, DI Input High Voltage	V_{IH}	2.7	3.1	3.5	V
CS, SCLK, DI Input Low Voltage	V_{IL}	1.7	2.1	2.5	V
CS, SCLK, DI Input Voltage Threshold Hysteresis	V_{Ihys}	0.8	1.0	1.2	V
CS, SCLK, DI Pull–Down Current, CS, SCLK, DI = VDDH to $V_{IL(min)}$	I_{SPI_PD}	10	20	50	µA
AC CHARACTERISTICS:					
SPI					
NOTES: MPC565 QSMCM/ SPI set for CPHA = 0 & CPOL = 0. *Assumes MPC565 SCLK rise and fall times of 30 ns, DO load = 200pF					
– Transfer Frequency	fop	dc		5.00	MHz
1 SCLK Period	tsck	200		–	ns
2 Enable Lead Time	tlead	105		–	ns
3 Enable Lag Time	tlag	50		–	ns
4 SCLK High Time*	tsckhs	70		–	ns
5 SCLK Low Time*	tsckls	70		–	ns
6 SDI Input Setup Time	tsus	16		–	ns
7 SDI Input Hold Time	ths	20		–	ns
8 SDO Access Time	ta	–		75	ns
9 SDO Disable Time	tdis	–		100	ns
10 SDO Output Valid Time	tvs	–		75	ns
11 SDO Output Hold Time	tho	0		–	ns
12 Rise Time (Design Information) (Note 1)	tro	–		30	ns
13 Fall Time (Design Information) (Note 1)	tfo	–		30	ns
14 CS Negated Time (Note 1)	tcsn	500		–	ns

NOTE:
1. Guaranteed by design but not production tested.

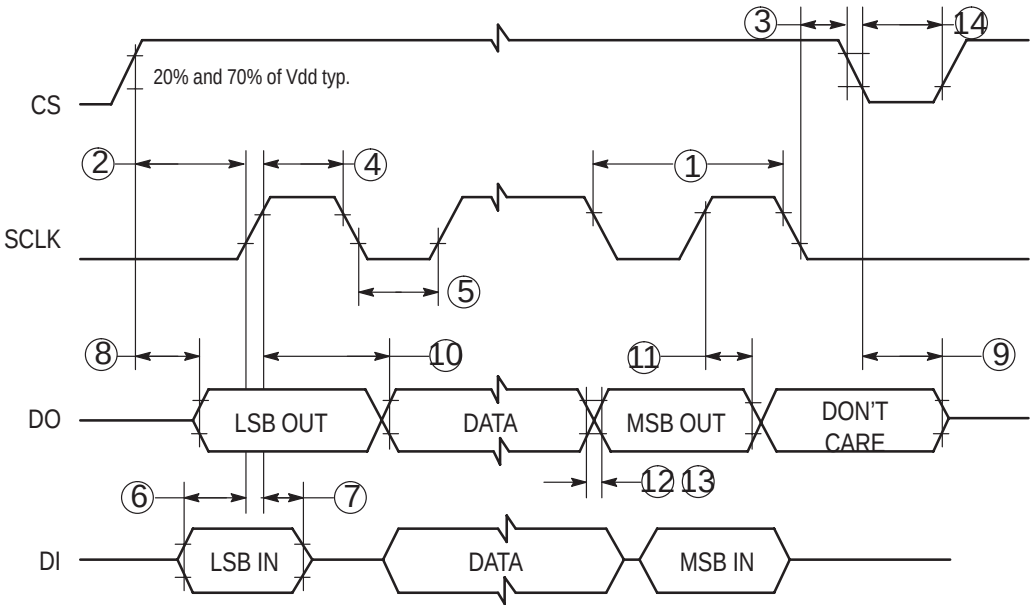

Figure 3. SPI Timing Diagram

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4. FUNCTIONAL DESCRIPTION

The 33394 is an integrated buck regulator/linear supply specifically designed to supply power to the Motorola MPC55x/MPC56x microprocessors. A detailed functional description of the Buck Regulator, Linear Regulators, Power Up/Down Sequences, Thermal Shutdown Protection, Can Transceiver Reset Functions and Reverse Battery Function are given below. Block diagram of the 33394 is given in Figure 1. The 33394 is packaged in a 44 pin HSOP, 54 pin SOICW and the 44 pin QFN.

4.1. Input Power Source (VBAT, KA_VBAT & VIGN)

The VBAT and KA_VBAT pins are the input power source for the 33394. The VBAT pins must be externally protected from vehicle level transients greater than +45 V and reverse battery. See typical application diagram in Figure 1. The VBAT pins directly supply the pre–regulator switching power supply. All power to the linear regulators (except VKAM in the power down mode) is supplied from VBAT through the switching regulator. VKAM power is supplied through VBAT input pins and switching regulator when the 33394 is awake. When the microprocessor is in a power down mode (no VDDH or VDDL supply), the current requirement on VKAM falls to less than 12 mA. During this period the VKAM current is supplied from the reverse battery protected KA_VBAT input.

The KA_VBAT supply pin is the power source to the Keep Alive Memory regulator (VKAM) in power down mode. Power is continuously supplied regardless of the state of the ignition switch (VIGN input). The KA_VBAT input is reverse battery protected but requires external load dump protection (refer to Figure 1).

The VIGN pin is used as a control input to the 33394. The regulation circuits will function and draw current from VBAT when VIGN is high (active) or REGON is high (active) or on CAN bus activity (WAKEUP active). To keep the VIGN input from floating, a 10kΩ pull–down resistor to GND should be used. The VIGN pin has a 3.0 V threshold and 1.0 volt of hysteresis. VIGN is designed to operate up to +26.5 volt battery while providing reverse battery and +45 volt load dump protection. The input requires ESD, and transient protection. See Figure 1 for external component required.

4.2. Switching Regulator Functional Description

A block diagram of the internal switching regulator is shown in Figure 4. The switching regulator incorporates circuitry to implement a Buck or a Buck/Boost regulator with additional external components. A high voltage, low $R_{DS(on)}$ power MOSFET is included on chip to minimize the external components required to implement a Buck regulator. The power MOSFET is a sense FET to implement current limit. For low voltage operation, a low side driver is provided that is capable of driving external logic level MOSFETs. This allows a switching regulator utilizing Buck/Boost topology to be implemented. Two independent control schemes are utilized in the switching regulator.

In Buck mode, voltage mode pulse–width modulation (PWM) control is used. The switcher output voltage divided by an internal resistor divider is sensed by an Error Amplifier and compared with the bandgap reference voltage. The PWM Comparator uses the output signal from the Error Amplifier as the threshold level. The PWM Comparator compares the sawtooth voltage from the Ramp Generator with the output signal from the Error Amplifier thus creating a PWM signal to the control logic block. The Error Amplifier inverting input and output are brought out to enable the control loop to be externally compensated. The compensation technique is described in paragraph **5.2.3. Buck Converter Feedback Compensation** in the Application Information section. In order to improve line rejection, feed forward is implemented in the ramp generator. The feed forward modifies the ramp slope in proportion to the VBAT voltage in a manner to keep the loop gain constant, thus simplifying loop compensation. At startup, a soft start circuit lowers the current limit value to prevent potentially destructive in–rush current.

In Boost mode, pulse–frequency modulation (PFM) control is utilized. The duty cycle is set to 75% and the switching action is stopped either by the Boost Comparator, sensing the switcher output voltage VPRE, or by the Current Limit circuit when the switching current reaches its predetermined limit value. This control method requires no external components. The selection of the control method is determined by the control logic based on the VBAT input voltage.

4.2.1. Switching Transistor (SW1)

The internal switching transistor is an n–channel power MOSFET. The $R_{DS(on)}$ of this internal power FET is approximately 0.25 ohm at +125°C. The 33394 has a nominal instantaneous current limit of 3.0 A (well below the saturation current of the MOSFET and external surface mounted inductor) in order to supply 1.2 A of current for the linear regulators that are connected to the VPRE pin (see Figure 1). The input to the drain of the internal N—channel MOSFET must be protected by an external series blocking diode, for reverse battery protection (see Figure 1).

4.2.2. Bootstrap Pin (BOOT)

An external bootstrap 0.1 µF capacitor connected between SW1 and the BOOT pin is used to generate a high voltage supply for the high side driver circuit of the buck controller. The capacitor is pre charged to approximately 10V while the internal FET is off. On switching, the SW1 pin is pulled up to VBAT, causing the BOOT pin to rise to approximately VBAT+10V — the highest voltage stress on the 33394.

4.2.3. External MOSFET Gate Drive (SW2G)

This is an output for driving an external FET for boost mode operation. Due to the fact that the gate drive supply voltage is VPRE the external power MOSFET should be a logic level device. It also has to have a low $R_{DS(on)}$ for acceptable efficiency. During buck mode, this gate output is held low.

4.2.4. Compensation (INV, VCOMP)

The PWM error amplifier inverting input and output are brought out to allow the loop to be compensated. The recommended compensation network is shown in Figure 18 and its Bode plot is in Figure 19. The use of external compensation components allows optimization of the buck converter control loop for the maximum bandwidth. Refer to the paragraph **5.2.3. Buck Converter Feedback Compensation** in the Application Information section for further details of the buck controller compensation.

4.2.5. Switching Regulator Output Voltage (VPRE)

The output of the switching regulator is brought into the chip at the VPRE pin. This voltage is required for both the switching regulator control and as the supply voltage for all the linear regulators.

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4.2.6. Switching Regulator Output Voltage Sense (VPRE_S)

This is the switching regulator output voltage sense input. The switcher output voltage VPRE is divided by an internal resistor divider and compared with the bandgap reference voltage (see Figure 4).

Refer to Section 5 Application Information for detailed description of the switching regulator operation.

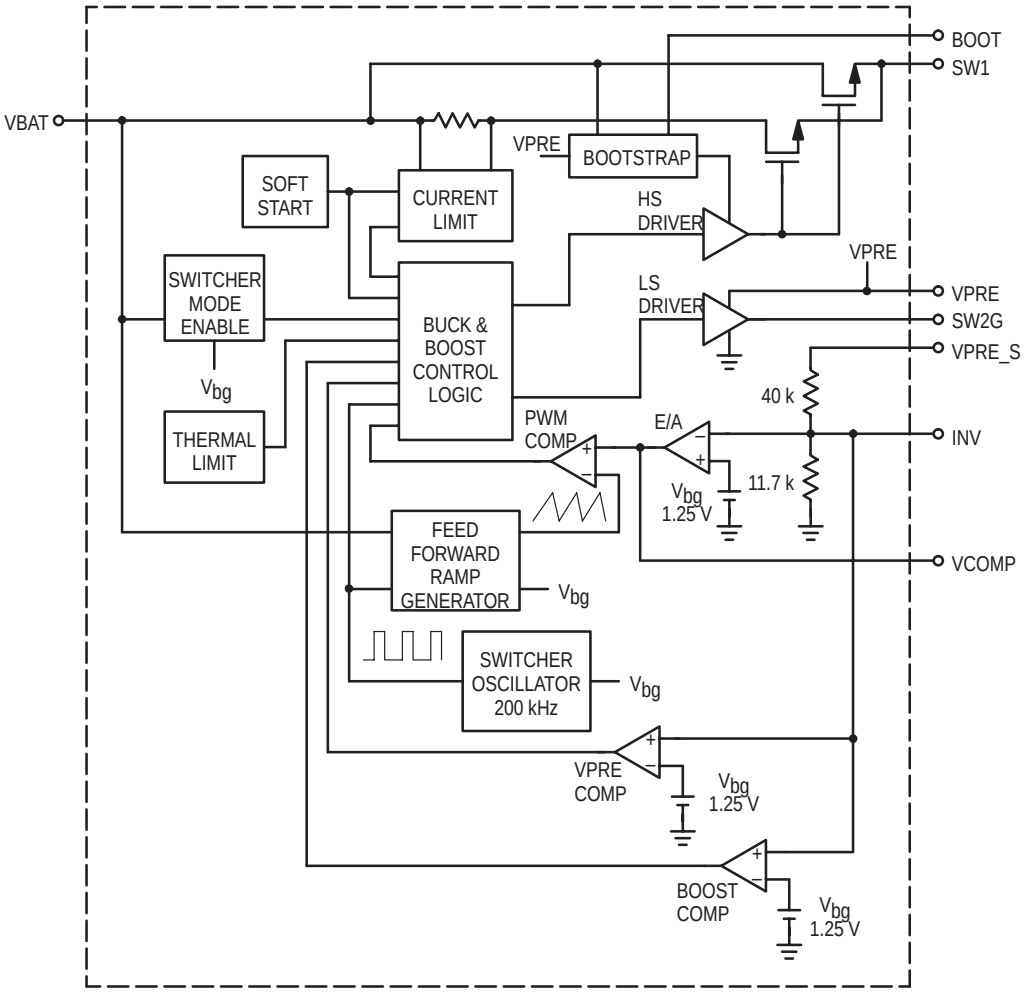

Figure 4. Switching Regulator Block Diagram

4.3. Voltage Regulator (VDDH)

The VDDH output is a linearly regulated +5.0 +/– 0.10V voltage supply capable of sourcing a maximum of 400 mA steady state current from VPRE (+5.6 V) for VBAT voltages from +4.0 V to +26.5 V (+45V transient). This regulator incorporates current limit short circuit protection and thermal shut down protection. The voltage output is stable under all load/line conditions. However, the designer must consider ripple and high frequency filtering as well as regulator response, when choosing external components. See Table 1 in the Applications Information section for recommended output capacitor parameters.

NOTE :

Backfeeding into the VDDH output can cause problems during the power up sequence. Refer to the Electrical Characteristics VDDH Regulator Section for the maximum allowed backfed current into the VDDH output.

4.4. Tracking Voltage Regulator (VPP)

This linearly regulated +5.0 V/+3.3 V (SPI selectable) voltage supply is capable of sourcing 150 mA of steady state current from VPRE (+5.6 V) for VBAT voltage from +4.0 V to +26.5 V (up to +45V transient). It tracks the VDDH or VDD3_3 output, and incorporates current limit short circuit protection and over temperature shut down protection. This output is intended for FLASH memory programming and includes a dedicated enable pin (VPP_EN). The regulator enable can also be controlled through the SPI interface but requires both the VPP_EN pin and the SPI bit (EN_VPP bit) to be high to enable. The selection of tracking VDDH or VDD3_3 is controlled by the VPP_V bit in the SPI. Logic “1” selects VDDH (default), logic “0” selects VDD3_3. The voltage output is stable under all load/line conditions. However, the designer must consider ripple and high frequency filtering as well as regulator response when choosing external components. See Table 1 for recommended output capacitor parameters.

The VPP tracking regulator should not be used in parallel with the VDDH regulator, because this arrangement can corrupt the proper power sequencing of the IC.

4.5. Tracking Voltage Regulator (VREFn)

The outputs of the VREF1, VREF2, VREF3 linear regulators are 100 mA at +5.0 V. They track the VDDH output. The power supplies are designed to supply power to sensors that are located external to the module. These regulators may be enabled or disabled via the SPI, which also provides fault reporting for these regulators. They are protected for short to

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battery (+18 V) and short to –2.0 V. Precautions must be taken to protect the VREF pins from exposure to transients. See Table 1 for recommended output capacitor parameters.

4.5.1. VREF Over Temperature Latch Off Feature

If either the VREF1, VREF2 or VREF3 outputs is shorted to ground for any duration of time, an over temperature shut down circuit disables the output source transistor once the local die temperature exceeds +150°C to +190°C. The output transistor remains off until the locally sensed temperature is 5°C to 20°C. below the trip off temperature. The output(s) will periodically turn on and off until either the die temperature decreases or until the fault condition is removed. If one of these outputs goes into over—temperature shutdown, it will not impact the operation of any of the other outputs (assuming that no other package thermal or VPRE current limit specifications are violated). Fault information is reported through the SPI communication interface (see Figure 8).

4.6. Voltage Regulator (VDD3_3)

This linearly regulated +3.3 V +/–0.06 V voltage supply is capable of sourcing 120 mA of steady state current from VPRE (+5.6 V) for VBAT voltage from +4.0 V to +26.5 V (+45V transient). This regulator incorporates current limit short circuit protection and thermal protection. When no external pass transistor is used the VDD3_3 and the VDD3_3FB pins must be shorted together — see Figure 22. The current capability of the VDD3_3 output can be increased by means of an external pass transistor — see Figure 1. When the external pass transistor is used the VDD3_3 internal short circuit current limit does not provide the short circuit protection. The voltage output is stable under all load/line conditions. However, the designer must consider ripple and high frequency filtering as well as regulator response when choosing external components. See Table 1 in the Applications Information section for recommended output capacitor parameters.

NOTE :

Backfeeding into the VDD3_3 output can cause problems during the power up sequence. Refer to the Electrical Characteristics VDD3_3 Regulator Section for the maximum allowed backfed current into the VDD3_3 output.

4.7. Voltage Regulator (VDDL)

The output voltage of the VDDL linear regulator is adjustable by means of an external resistor divider.

This linearly regulated +/–2% core voltage supply uses an external pass transistor and is capable of sourcing 40 mA base drive current typically (see application circuit, Figure 1) of steady state current. The collector of the external NPN pass transistor is connected to VPRE (+5.6 V) for a VBAT voltage from +7.5 V to +26.5 V (+45V transient). The voltage output is stable under all load/line conditions. However, the designer must consider ripple and high frequency filtering as well as regulator response when choosing external components. Also, the dynamic load characteristics of the microprocessor, relative to CPU clock frequency changes must be considered. An additional external pass transistor, for VDDL regulation in the Boost mode, can be added between protected battery voltage (see Figure 1) and VDDL, with its base driven by VDDL_X. In that arrangement the 33394's core voltage supply operates over the whole input voltage range VBAT = +4.0 V to +26.5 V (up to +45V transient). See Table 1 in the Applications Information section for recommended output capacitor parameters.

NOTES:

1. The use of an EXTERNAL pass device allows the power dissipation of the 33394 to be reduced by approximately 50% and thereby allows the use of a thermally efficient package such as an HSOP 44 or QFN 44. The base drive control signal (VDDL_B) is provided by on chip circuitry. The regulated output voltage sense signal is fed back into the on chip differential amplifier through pin VDDL_FB. The collector of this external pass device should be connected to VPRE to minimize power dissipation and adequately supply 400 mA. Proper thermal mounting considerations must be accounted for in the PCB design.

2. Backfeeding into the VDDL output can cause problems during the power up sequence. Refer to the Electrical Characteristics VDDL Regulator Section for the maximum allowed backfed current into the VDDL output.

4.8. Keep–Alive/Standby Supply (VKAM)

This linearly regulated Keep Alive Memory voltage supply tracks the VDDL (+1.25 V to +3.3 V) core voltage, and is capable of sourcing 50 mA of steady state current from VPRE during normal microprocessor operation and 12 mA through KA_VBAT pin during stand–by/sleep mode. The VKAM regulator output incorporates a current limit short circuit protection. The output requires a specific range of capacitor values to be stable under all load/line conditions. See Table 1 in the Applications Information section for recommended output capacitor parameters.

NOTE :

The source current for the VKAM supply output depends on the sleep/wake state of the 33394.

4.9. Switched Battery Output (VSEN)

This is a saturated switch output, which tracks the VBAT and is capable of sourcing 125 mA of steady state current from VBAT. This regulator will track the voltage VBAT to less than 200 mV, and its output voltage is clamped at +17 V. The gate voltage of the internal N—channel MOSFET is provided by a charge pump from VBAT. There is an internal gate–to–source voltage clamp. This regulator is short circuit protected and has independent over—temperature protection. If this output is shorted and goes into thermal shutdown, the normal operation of all other voltage outputs is not impacted. This output is controlled by the SPI VSEN bit.

NOTE:

A short to VBAT on VREF1, VREF2, VREF3 or VSEN will not result in additional current being drawn from the battery under normal (+8 V to +18 V) voltage levels. Under jumpstart condition (VBAT = +26.5 V) and during load dump condition, the device will survive this condition, but additional current may be drawn from the battery.

4.9.1. VSEN Over Temperature Latch Off Feature

If the VSEN output is shorted to ground for any duration of time, an over temperature shut down circuit disables the output source transistor once the local die temperature exceeds +150°C to +190°C. The output transistor remains off until the locally sensed temperature drops 5°C to 20°C below

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the trip–off temperature. The output will periodically turn on and off until either the die temperature decreases or until the fault condition is removed. If the VSEN output goes into over—temperature shutdown, it does not impact the operation of any of the other outputs (assuming that no other package thermal or VPRE current limit specifications are violated). Fault information is reported through the SPI communication interface (see Figure 8).

4.10. Resets To Microprocessor

/PORESET – Power On Reset, /PRERESET — Pre Reset, /HRESET– Hardware Reset. All the Reset pins are open drain 'active low' outputs, capable of sinking 1.0 mA current and able to withstand +7.0 V. See Figure 1 and Figure 20 for recommended pull–up resistor values and their connection.

The /PORESET pin is pulled up to the VKAM voltage by a pull up resistor. It is connected to the microprocessor Power On Reset (POR) pin, and is normally high. During initial battery connect the /PORESET is held to ground by the 33394. After the VKAM supply is in regulation and an internal 10 ms timer has expired, the /PORESET is released. If VKAM goes out of regulation the device will first pull the /PORESET and /PRERESET followed by a 0.7 µs delay then /HRESET. By /HRESET low VDDH, VDD3_3 and VDDL will start a power down sequence. When the fault is removed a standard power up sequence is initiated. The VKAM linear regulator output must be out of regulation for greater than 20 µs before /PORERSET and /PRERESET (with /HRESET 0.7 µs delayed) are pulled low. If a fault occurs on VKAM in the Key–Off Mode (when the VIGN is off) and the fault is then removed the VKAM will regulate but /PORESET will not be released until Key–On (asserting VIGN pin) allows the 10 ms timer to run.

The Reset signals (/PRERESET, /HRESET) are not asserted when the 33394 enters Sleep Mode by asserting the /SLEEP pin. When exiting out of Sleep Mode the 33394 asserts the Resets (/PRERESET, /HRESET) during the power up sequence.

The /PRERESET and /HRESET pins are pulled up to the VKAM (see Figure 1) or to VDDL (see Figure 20). Refer to section **5. Application Information**, paragraph **5.3. Selecting Pull–Up Resistors** for detailed description of these two connection scenarios. The 33394 monitors the main supply voltages VDDH, VDD3_3 and VDDL. If any of these voltages falls out of regulation limits the /PRERESET will be pulled down followed by the /HRESET after 0.7 µs delay, and the power down sequence will be initiated. There are several different scenarios how to connect the /PRERESET and /HRESET pins to the microprocessor. Typically the /PRERESET pin will be connected to the IRQ0 pin of the microprocessor, and the /HRESET to the microprocessor /HRESET pin (see Figure 5). The VDDH, VDD3_3 and VDDL linear regulator outputs must be out of regulation for greater than 20 µs before /PRERESET (with /HRESET 0.7 µs delayed) are pulled low.

4.11. Hardware Reset Timer (HRT)

The HRT pin is used to set the delay between VDDH, VDD3_3 and VDDL active and stable and the release of the /HRESET and /PRERESET outputs. An external resistor and capacitor is used to program the timer. To minimize quiescent current during power down modes, the RC timer current should be drawn from one of the VDD supplies (see Figure 1). The threshold on the HRT pin has zero temperature coefficient and is set at 2.5 V.

4.12. Power Up/Down Sequencing

The 33394 power up sequence is specifically designed to meet the power up and power down requirements of the MPC565 microprocessor. The MPC565 processor requires that VDDH remain within 3.1 volts of VDDL during power up and can not lag VDDL by more than 0.5 volts. This condition is met by the 33394 regardless of load impedance. It is critical to note that the 33394 under normal conditions is designed to supply VKAM prior to the power up sequence on VDDH, VDD3_3 and VDDL. During power up and power down sequencing /PRERESET and /HRESET are held low. Power up and power down sequencing is implemented in six steps. During this process the reference voltage for VDDH, VDD3_3 and VDDL is ramped up in six steps. Minimum power up/down time is dependent on the internal clock and is 800 µs. Maximum power up/down time is also dependent on load impedance. During the power up/down cycle, voltage level requirements for each step of VDDH, VDD3_3 and VDDL must be met before the supply may advance to the next voltage level. Hence VDDH and VDDL will remain within the 3.1/0.5 V window. Figure 6 illustrates a typical power up and down sequence.

4.13. Regulator Enable Function (REGON)

This feature allows the microcontroller to select the delayed shut down of the 33394 device. It holds off the activation of the Reset signals, to the microcontroller, after the VIGN signal has transitioned and signals the request to shutdown the VDDH, VDD3_3, VDDL, VSEN and the VREFn supplies. This allows the microcontroller to delay a variable amount of time, after sensing that the VIGN signal has transitioned and signaled the request to shutdown the regulated supplies. This time can be used to store data to EPROM memory, schedule an orderly shutdown of peripherals, etc. The microcontroller can then drive the REGON signal, to the 33394, to the low logic state, to turn off the regulators (except for the VKAM supply).

4.14. Regulator Shutdown Function (/SLEEP)

This feature allows for an external control element (e.g. microprocessor) to shut down the 33394 regulators, even if the VIGN signal (or REGON) is active, by asserting the /SLEEP pin from high to low (falling edge transition). In this case the 33394 initiates the power down sequence, but the Reset signals (/PRERESET, /HRESET) are not asserted. This allows the microprocessor to continue to execute code when it is supplied only from the Keep Alive supply VKAM. When the microprocessor exits sleep state by pulling /SLEEP pin high the Resets (/PRERESET, /HRESET) are asserted during the power up sequence.

The /SLEEP pin has an internal pull down, therefore when its functionality is not used this pin can be either pulled up to VKAM, VBAT, pulled down to ground or left open.

The /SLEEP pin should not be pulled up to VDDH.

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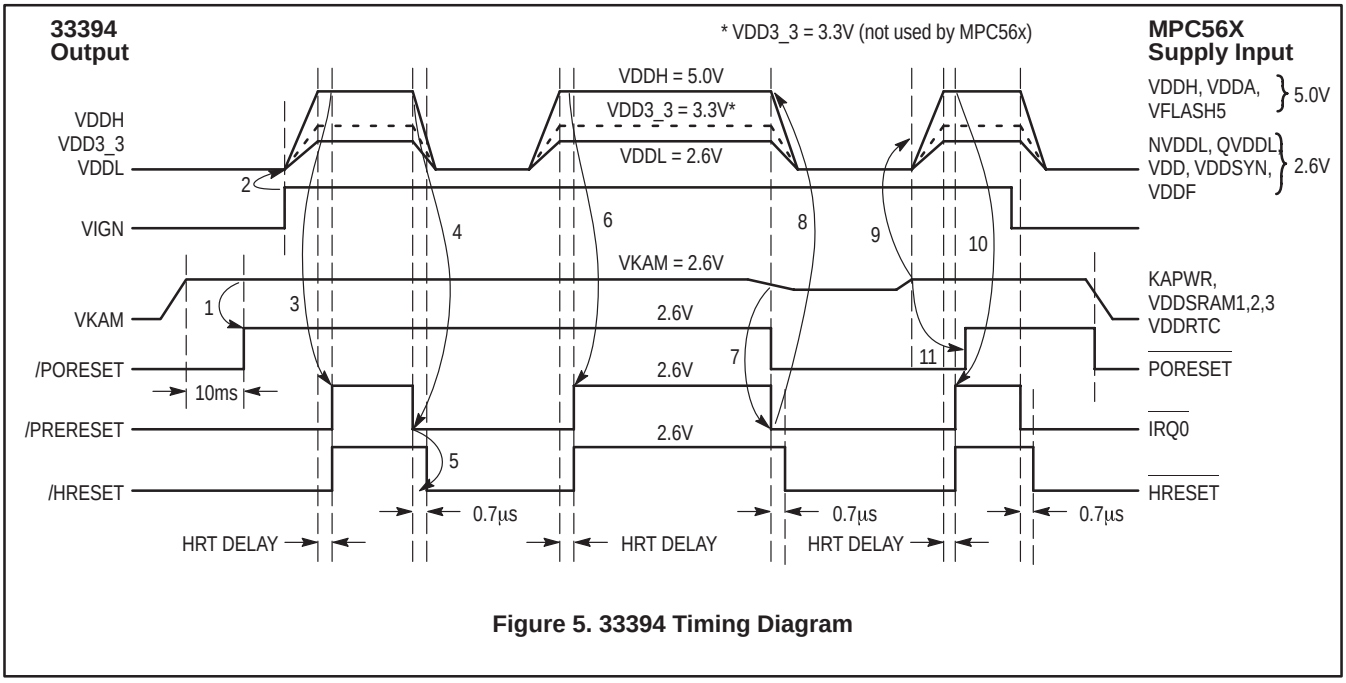

Figure 5. 33394 Timing Diagram

1 Module connected to the battery, VKAM starts to regulate, /PORESET is released after VKAM is in regulation for 10 ms.
2 VIGN is applied, 33394 starts power up sequence.
3 VDDH, VDD3_3, VDDL are stable and in regulation before /PRERESET and /HRESET are released (with a HRT delay programmable by an external capacitor and resistor, HRT pin).
4 Any of VDDH, VDD3_3, VDDL voltages out of regulation initiate /PRERESET asserted. Power down sequence initiated.
5 /HRESET is asserted 0.7 µs after /PRERESET
6 When fault is removed and VDDH, VDD3_3, VDDL are in regulation, the /PRERESET and /HRESET outputs are released (with an HRT delay).
7 When VKAM goes out of regulation limits (4% below its nominal value), /PORESET, /PRERESET and /HRESET (/HRESET with 0.7 µs delay) are asserted – see Note 1.
8 33394 initiates power down sequence.
9 Fault on VKAM removed, the 33394 initiates the start up sequence.
10 When VDDH, VDD3_3, VDDL are in regulation again, the /PRERESET and /HRESET outputs are released (with an HRT delay).
11 /PORESET is released with a 10 ms delay after the fault on VKAM was removed.

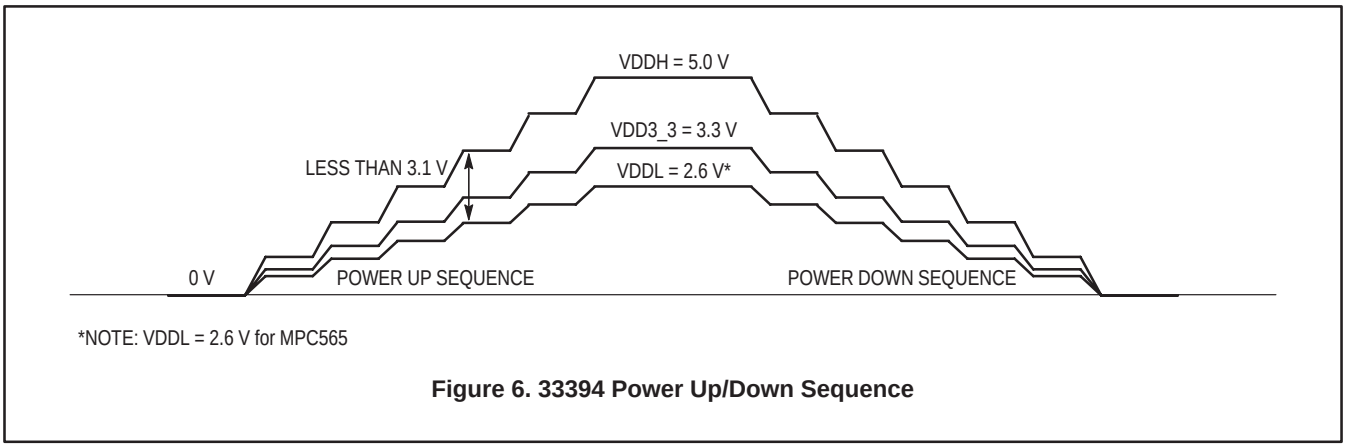

Figure 6. 33394 Power Up/Down Sequence

* VKAM voltage level for MPC55x devices is 3.3 V and for MPC56x devices is 2.6 V.

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4.15. SPI Interface to Microcontroller (Serial Peripheral Interface)

The pins specified for this function are: DI (Data Input), DO (Data Output), CS (Chip Select) and SCLK. Refer to Figure 3 for the 33394 SPI timing information. The delay, which is needed from CS leading edge active to the first SCLK leading edge transition (0 to 1) is approximately 125 ns. The SCLK rate is a maximum of 5.0 MHz. The SPI function will provide control of such 33394 features as VREFn regulator turn on/off, VREFn fault reporting and CAN wake up feature activation. Refer to Figure 7 & Figure 8 for the data and status bit assignments for the 16 bit SPI data word exchange.

4.15.1. CS (Chip Select) Pin

The system MCU selects the 33394 to be communicated with through the use of the CS pin. Whenever the pin is in a logic high state, data can be transferred from the MCU to the 33394 and vice versa. Clocked—in data from the MCU is transferred to the 33394 shift register and latched in on the falling edge of the CS signal. On the rising edge of the CS signal, output status information is transferred from the output status register into the device's shift register. Whenever the CS pin goes to a logic high state, the DO pin output is enabled allowing information to be transferred from the 33394 to the MCU. To avoid any spurious data, it is essential that the transition of the CS signal occur only when SCLK is in a logic low state.

4.15.2. SCLK (System Clock) Pin

The shift clock pin (SCLK) clocks the internal shift registers of the 33394. The serial input (DI) data is latched into the input shift register on the rising edge of the SCLK. The serial output pin (DO) shifts data information out of the shift register also on the rising edge of the SCLK signal. It is essential that the SCLK pin be in a logic low state whenever the chip select pin (CS) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin is commanded to a low logic state as long as the device is not accessed (CS in logic low state). When CS is in a logic low state, any signal at the SCLK and DI pin is ignored and the DO is tri—stated (high impedance).

4.15.3. DI (Data Input) Pin

The DI pin is used for serial data input. This information is latched into the input register on the rising edge of SCLK. A logic high state present on DI will program a specific function (see Figure 7 for the data bits assignments for the 16 bit SPI data word exchange.). The change will happen with the falling edge of the CS signal. To program the specific function of the 33394 a 16 bit serial stream of data is required to be entered into the DI pin starting with LSB. For each rising edge of the SCLK while CS is logic high, a data bit instruction is loaded into the shift register per the data bit DI state. The shift register is full after 16 bits of information have been entered. To preserve data integrity, care should be taken to not transition DI as SCLK transitions from a low to high logic state.

4.15.4. DO (Data Output) Pin

The serial output (DO) pin is the output from the shift register. The DO pin remains tri—state until the CS pin goes to a logic high state. See Figure 8 for the status bits assignments for the 16–bit SPI data word exchange. The CS positive transition will make LSB status available on DO pin. Each successive positive SCLK will make the next bit status available. The DI/DO shifting of data follows a first—in—first—out protocol with both input and output words transferring the Least Significant Bit (LSB) first.

33394 SPI Registers:

Serial Input Data/Control

Default Value	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								

Bit Definitions:

Bit 15 to 8 = 0

Default Value	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0 (LSB)
Name	WKUP	CAN_EN	VPP_V	EN_VPP	VSEN	VREF3	VREF2	VREF1

Bit Definitions:

Bit 7 — WKUP: WAKEUP activation. WKUP = 1: WAKEUP pin will signal CAN bus activity
Bit 6 — CAN_EN: Enables CAN receiver, will draw small current during power off
Bit 5 — VPP_V: Set VPP reference to 5V (1) or 3.3V (0), default is 5V
Bit 4 — EN_VPP: – Used to turn the VPP regulator off and on from the MCU
Bit 3 — VSEN: – Used to turn the VSEN regulator off and on from the MCU
Bit 2 — VREF3: – Used to turn the VREF3 regulator off and on from the MCU
Bit 1 — VREF2: – Used to turn the VREF2 regulator off and on from the MCU
Bit 0 — VREF1: – Used to turn the VREF1 regulator off and on from the MCU

Figure 7. SPI Input Data/ Control Register

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33394 SPI Registers:
Serial Output Data/Status

Default Value	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Name								

Bit Definitions:
Bit 15 to 8 = 0

Default Value	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0 (LSB)
Name	VSEN–T	VREF3–T	VREF2–T	VREF1–T	VSEN–I	VREF3–I	VREF2–I	VREF1–I

Bit Definitions:
Bit 7 — VSEN–T: – Will be set (1), if a thermal limit occurred since last SPI data transfer
Bit 6 — VREF3–T: – Will be set (1), if a thermal limit occurred since last SPI data transfer
Bit 5 — VREF2–T: – Will be set (1), if a thermal limit occurred since last SPI data transfer
Bit 4 — VREF1–T: – Will be set (1), if a thermal limit occurred since last SPI data transfer
Bit 3 — VSEN–I: – Will be set (1), if a current limit condition exists
Bit 2 — VREF3–I: – Will be set (1), if a current limit condition exists
Bit 1 — VREF2–I: – Will be set (1), if a current limit condition exists
Bit 0 — VREF1–I: – Will be set (1), if a current limit condition exists

NOTES: # individual thermal limit latch will clear on the trailing edge of the SPI CS signal

Figure 8. SPI Output Data/ Status Register

4.16. CAN Transceiver

The CAN protocol is defined in terms of 'dominant' and 'recessive' bits. When the digital input (CANTXD) is a logic "0" (negated level, dominant bit), CANH goes to +3.5 V (nominal) and CANL goes to +1.5 V (nominal). The digital output will also be negated. When the digital input is logic "1" (asserted level, recessive bit), CANH and CANL are set to +2.5 V (nominal). The corresponding digital output is also asserted.

4.16.1. CAN Network Topology

There are two 120 Ω (only two), terminations between the CANH and CANL outputs. The majority of the time, the module controller will contain one of the terminations. The other termination should be as close to the other "end" of the CAN Bus as possible. The termination provides a total of 60 Ω differential resistive impedance for generation of the voltage difference between CANH and CANL. Current flows out of CANH, through the termination, and then through CANL and back to ground. The CAN bus is not defined in terms of the bus capacitance. A filter capacitor of 220 pF to 470 pF may be required. The maximum capacitive load on the CAN bus is then 15 nF (not a lumped capacitance but distributed through the network cabling). Refer to Figure 9.

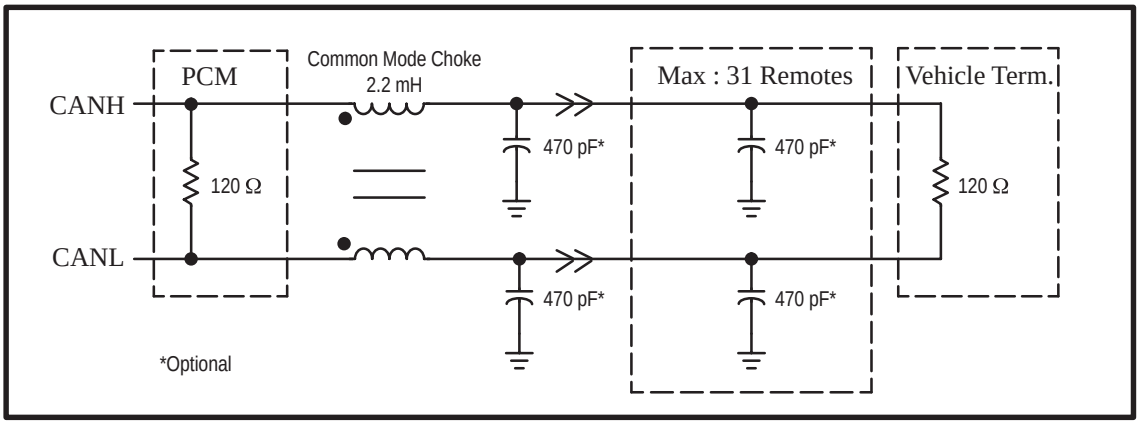

Figure 9. CAN Load Characteristics

4.16.2. CAN Transceiver Functional Description

A block diagram of the CAN transceiver is shown in Figure 10. A summary of the network topology is shown in Figure 9. The transceiver has wake up capability controlled by the state of the SPI bit WKUP. This allows 33394 to enter a low power mode and be awakened by CAN bus activity. When activity is sensed on the CAN bus pins, the 33394 will perform a power up sequence and will provide the microprocessor with indication (WAKEUP pin high) that wake up occurred from a CAN message. The 33394 may be placed back in low quiescent mode by pulling the /SLEEP pin from high to low.

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The Wake–up function can be disabled through SPI by setting the WKUP bit to 0.

The CAN transceiver of the 33394 is designed for communications speeds up to 1.0 Mbps. The use of a common mode choke may be required in some applications. When the 33394 CAN transceiver physical interface is not used in the system design, the CAN bus driver pins CANH and CANL should be shorted together.

4.16.3. CANH

CANH is an output driver stage that sources current on the CANH output. It's output follows CANL, but in the opposite polarity. The output is short circuit protected. In the event that battery or ground is lost to the module, the CANH transmitter's output stage is disabled.

4.16.4. CANL

CANL is an output driver stage that sinks current on the CANL output. The sink type output is short circuit protected. In the event that battery or ground is lost to the module, the CANL transmitter's output stage is disabled.

4.16.5. CANTXD

CANTXD input comes from the microcontroller and drives that state of the CAN bus pins, CANH and CANL. A logic '0' input drives the outputs to a differential (dominant) voltage, where the CANH output is +3.5 V and the CANL output is +1.5 V. A logic '1' input drives the outputs to their idle (recessive) state, where the CANH and CANL outputs are +2.5 V. An internal pull–up to VDDH shall guarantee a logic "1" input level if this input is left open. On power–up, or in the event of a thermal shutdown, this input must be toggled high and then low to clear the thermal fault latch. The faulted CAN bus output(s) will remain disabled until the thermal fault latch is cleared. The CAN bus data rate is determined by the data rate of CANTXD.

4.16.6. CANRXD

This is a CMOS compatible output used to send data from the CAN bus pins, CANH and CANL, to the microprocessor. When the voltage differential between CANH and CANL is under the differential input voltage threshold (recessive state), CANRXD is logic '1'. When the voltage differential between CANH and CANL is over the voltage threshold (dominant state), CANRXD is logic '0'. In standby mode, input voltage threshold remains the same. There is a minimum of 0.1 V of hysteresis between the high and low (and vice versa) transition points.

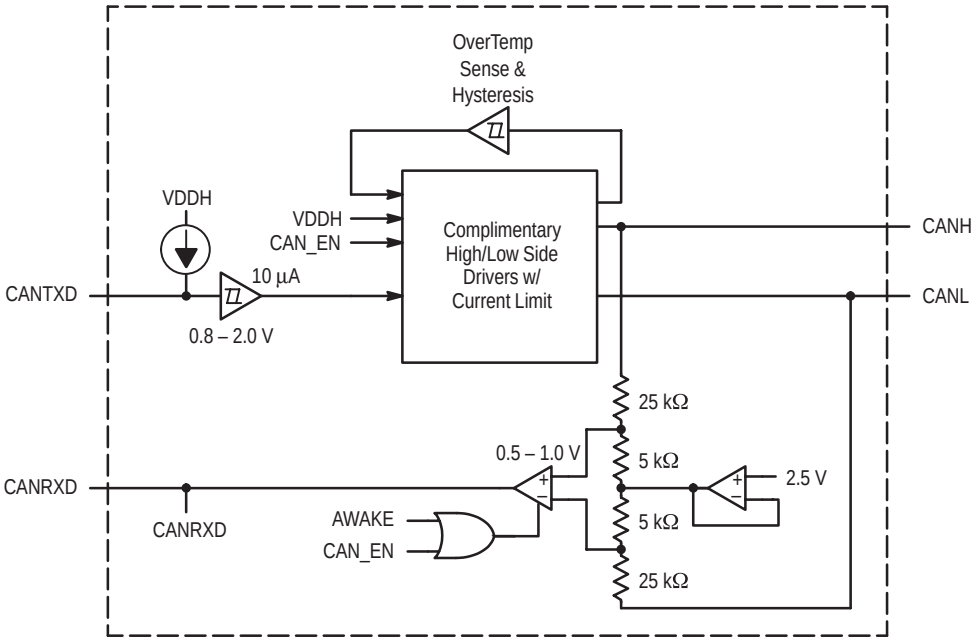

Figure 10. CAN Transceiver Block Diagram

4.16.7. CAN Over Temperature Latch Off Feature

If the CANH or CANL output is shorted to ground or battery for any duration of time, an over temperature shut down circuit disables the output stage. The output stage remains latched off until the CANTXD input is toggled from a logic '1' to a logic '0' to clear the over temperature shutdown latch. Thermal shutdown does not impact the remaining functionality of the IC.

4.16.8. CAN Loss of Assembly Ground

The definition of a loss of ground condition at the device level is that all pins of the IC (excluding transmitter outputs) will see very low impedance to VBAT. The loss of ground is shown on the module level in Figure 11. The nomenclature is suited to a test environment. In the application, a loss of ground condition results in all I/O pins floating to battery voltage. In this condition, the CAN bus must not source enough current to corrupt the bus.

4.16.9. CAN Loss of Assembly Battery

The loss of battery condition at the IC level is that the power input pins of the IC see infinite impedance to the battery supply voltage (depending upon the application) but there is some undefined impedance looking from these pins to ground. In this condition, the CAN bus must not sink enough current to corrupt the bus. Refer to Figure 12.

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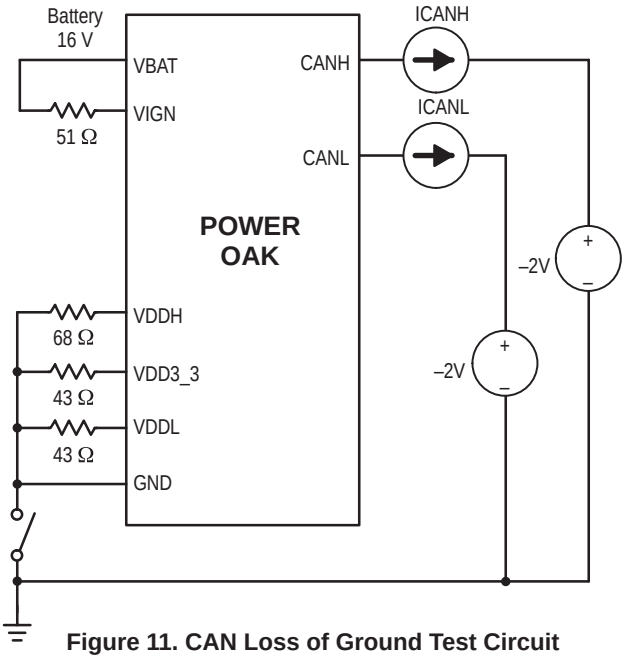

Figure 11. CAN Loss of Ground Test Circuit

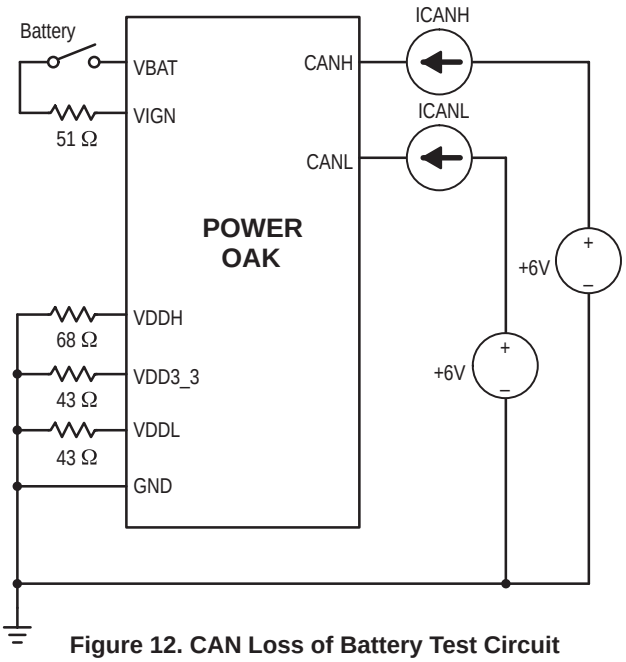

Figure 12. CAN Loss of Battery Test Circuit

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5. APPLICATION INFORMATION

This section provides information on external components that are required by the 33394. The IC is designed to operate in an automotive environment. Conducted immunity and radiated emissions requirements have been addressed during the design. However, the IC requires some external protection.

Protection is required for all pins connected directly to battery. The module designer should use an MOV or another transient voltage suppressor in all cases, when the load dump transition exceeds + 45 volts with respect to ground. Protection should also include a reverse battery protection diode (or relay) and input filter. This is required to protect the 33394 from ESD and +/– 300V ignition transients. Typical configurations are shown in Figure 1. Outputs and inputs connected directly to connector pins require module level ESD protection.

5.1. Selecting Components for Linear Regulators

The output capacitor of the linear regulator serves two different purposes. It maintains the linear regulator loop stability, and it provides an energy reservoir to supply current during very fast load transients. This is especially true when supplying highly modulated loads like microcontrollers and other high–speed digital circuits. Due to the limited bandwidth of the linear regulators, the output capacitor is selected to limit the ripple voltage caused by these abrupt changes in the load current. During the fast load current transients, the linear regulator output capacitor alone controls the initial output voltage deviation. Hence, the output capacitor's equivalent series resistance (ESR) is the most critical parameter.

The outputs, which do not experience such severe conditions (the VREF e.g.), use the output capacitor mainly for stability purpose, and therefore its capacitance value can be significantly smaller. The typical output capacitor parameters are: C = 1.0 µF; ESR = 2.0 ohms. When a ceramic 1 µF capacitor is used, the ESR can be provided by a discrete serial resistor (see Figure 20).

The following example shows how to determine the output capacitance for a heavily loaded output supplying digital circuits.

5.1.1. Selecting the Output Capacitor Example:

The output capacitance must be selected to provide sufficiently low ESR. The selected capacitor must have an adequate voltage, temperature and ripple current rating for the particular application.

In order to calculate the proper output capacitor parameters, several assumptions will be made.

1) During the very fast load current transients, the linear regulator can not supply the required current fast enough, and therefore for a certain time the entire load current is supplied by the output capacitor. 2) The capacitor's equivalent series inductance (ESL) is neglected. These assumptions can greatly simplify the calculations, and are reasonable for most of practical applications. Then the ESR of the output capacitor has to satisfy the following condition:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O}$$

Where:

ΔVo is the maximum allowed linear regulator voltage drop caused by the load current transient.

ΔIo is the maximum current transient, which can occur due to the abrupt step in the linear regulator load current.

In this example the VDDH output with the 400 mA load step is considered with the maximum voltage drop of 100mV. This gives the output capacitor's maximum ESR value of:

$$ESR = \frac{100\ mV}{400\ mA} = 250\ m\Omega$$

This level of ESR requires a relatively large capacitance. In order to maintain the linear regulator stability and to satisfy large load current steps requirements the solid tantalum capacitor 100µF/10V with ESR = 200 mΩ. One device that meets these requirements is the TPSC107K010S020 tantalum capacitor from the AVX Corporation.

$$\Delta V_{ESR} = ESR \times \Delta I_O = 200\ m\Omega \times 400\ mA = 80\ mV$$

In the next step, the voltage drop associated with the capacitance can be calculated:

$$\Delta V_C = \frac{\Delta I_O \times \Delta t}{C} = \frac{0.4\ A \times 5\ \mu s}{100\ \mu F} = 20\ mV$$

Where:

C is the output capacitance.

Δt is the linear regulator response time.

ΔI_O is the maximum current transient, which can occur due to the abrupt step in the linear regulator load current.

Assuming that the capacitor ESL is negligible, the total voltage drop in the voltage regulator output caused by the current fast transient can be calculated as:

$$\Delta V_{total} = \Delta V_{ESR} + \Delta V_C = 80\ mV + 20\ mV = 100\ mV$$

A ceramic capacitor with capacitance value 10nF should be placed in parallel to provide filtering for the high frequency transients caused by the switching regulator.

Properly sized decoupling ceramic capacitor close to the microprocessor supply pin should be used as well. Table 1 shows the suggested output capacitors for the 33394 IC linear regulator outputs.

Other factors to consider when selecting output capacitors include key off timing for memory retention. Though the VKAM is not a heavily loaded output, the VKAM output capacitor has to have a sufficiently large capacitance value to supply current to the microcontroller for a certain time after battery voltage is disconnected.

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Table 1. Linear Regulator Output Capacitor Examples

Output	SMD tantalum	
	Value/Rating	Part n. (AVX Corp.)
VDDH	100uF/10V	TPSC107K010S0200
VPP	33uF/10V	TPSB336K010S0650
VDD3_3	68uF/6.3V	TPSC686K006S0200
VDDL	100uF/6.3V	TPSC107K006S0150
VREFx	10uF/16V	THJB106K016S
VKAM*	100uF/6.3V	TPSC107K006S0150

5.2. Switching Regulator Operation

The 33394 switching regulator circuit consists of two basic switching converter topologies. One is the typical voltage mode PWM step–down or buck regulator, which provides pre–regulated VPRE voltage (+5.6 V) during normal operating conditions.

During cold start–up, when the car battery is weak, the input voltage for the 33394 can fall below the lower operating limit of the step–down converter. Under such conditions, the step–up or boost converter provides the required value of the VPRE voltage. The following paragraphs describe the basic principles of the two converters operation.

Buck Mode

One switching cycle of the step–down converter operation has two distinct parts: the power switch on state and the off state. When the power switch is on, one inductor terminal is connected to the input voltage Vin, and the other inductor terminal is the output voltage V_O. During this part of the switching period the rectifier (catch diode) is back biased, and the current ramps up through the inductor to the output:

$$i_{L(on)} = \frac{(V_{in} - V_O) \times t_{on}}{L}$$

Where:

t_{on} is the on–time of the power switch.

V_{in} is the input voltage.

V_O is the output voltage.

$i_{L(on)}$ is the inductor current during the on–time.

L is the inductance of the inductor L.

During the on time, current ramping through the inductor stores energy in the inductor core.

During the off time of the power switch, the input voltage source Vin is disconnected from the circuit. The energy stored in the core forces current to continue to flow in the same direction, the rectifier is forward biased and the inductor input voltage is clamped one forward diode drop below ground. The inductor current during the off time is:

$$i_{L(off)} = \frac{(V_O - V_{fwd}) \times t_{off}}{L}$$

Where:

t_{off} is the off–time of the power switch.

$i_{L(off)}$ is the inductor current during the off time.

V_{fwrd} is forward voltage drop across the rectifier.

During the steady state operation $i_{L(on)} = i_{L(off)} = \Delta I_L$, and

$V_{in}/V_O = d$

Where:

d is the duty cycle, and $d = t_{on}/T$.

T is switching period, T = 1/f.

f is the frequency of operation.

Two relations give the ripple voltage in the output capacitor C_O. The first describes ripple voltage caused by current variation upon the output capacitance C_O:

$$Vpp_{Co} = \frac{\Delta I_L}{8Co \times f}$$

The other is caused by current variations over the output capacitor equivalent series resistance ESR:

$$Vpp_{ESR} = \Delta I_L \times R_{ESR}$$

Practically, the ESR contributes predominantly to the buck converter ripple voltage:

$V_{ppESR} >> V_{ppCo}$

The inductor peak current can be calculated as follows:

$$Ipk_L = I_o + \frac{1}{2}\Delta I_L$$

Where:

I_o is the average output current.

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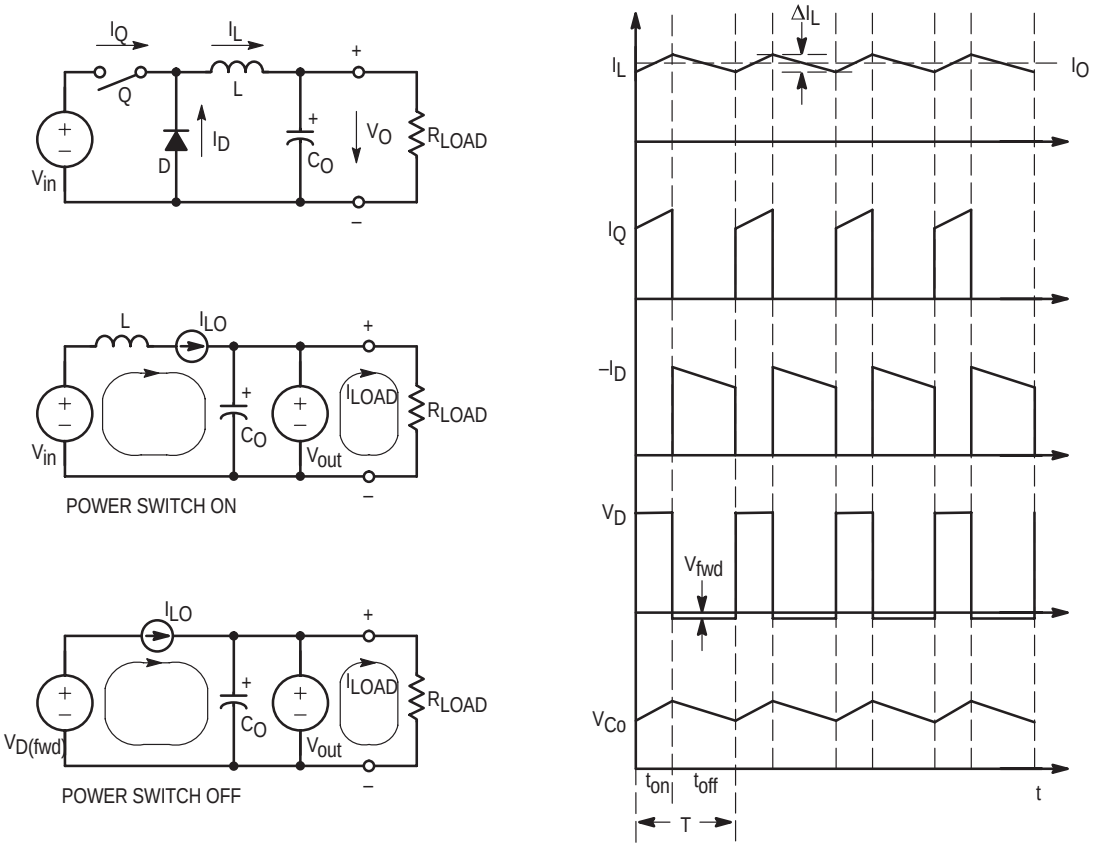

Figure 13. Basic Buck Converter Operation and its Waveforms

Boost Mode

The operation of the boost converter also consists of two parts, when the power switch is on and off. When the power switch turns on, the input voltage source is placed directly across the inductor, and the current ramps up linearly through the inductor as described by:

$$i_{L(on)} = \frac{V_{in} \times t_{on}}{L}$$

Where:

t_{on} is the on–time of the power switch.

V_{in} is the input voltage.

$i_{L(on)}$ is the inductor current during the on–time.

L is the inductance of the inductor L.

The current ramping across the inductor stores energy within the core material. In order to maintain steady–state operation, the amount of energy stored during each switching cycle, times the frequency of operation must be higher (to cover the losses) than the power demands of the load:

$$P_{sto} = \frac{1}{2} L I^2_{pk} \times f > P_{out}$$

When the power switch turns off again, the inductor voltage flies back above the input voltage and is clamped by the forward biased rectifier at the output voltage.

The current ramps down through the inductor to the output until the new on time begins or, in case of discontinuous mode of operation, until the energy stored in the inductor core drops to zero.

$$i_{L(off)} = \frac{(V_o - V_{in}) \times t_{off}}{L}$$

Where:

t_{off} is the off–time of the power switch.

V_o is the output voltage.

During the steady state operation $i_{L(on)} = i_{L(off)} = \Delta I_L$, and

$$d = \frac{V_o - V_{in}}{V_o}$$

Where:

d is the duty cycle, and $d = t_{on}/T$.

T is switching period, T = 1/f.

f is the frequency of operation.

The ripple voltage of the boost converter can be described as:

$$Vpp_{Co} = \frac{I_o}{C_o} \times \frac{(V_o - V_{in})}{V_o \times f}$$

Where:

V_{ppCo} is the ripple caused by output current.

The portion of the output ripple voltage caused by the ESR of the output capacitor is:

$$Vpp_{ESR} = (I_o \times \frac{V_o}{V_{in}} + \frac{1}{2}\Delta I_L) \times R_{ESR}$$

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Where I_O is the average output current.

The inductor peak current is given by the following equation:

$$Ipk_L = I_o \times \frac{V_o}{V_{in}} + \frac{1}{2}\Delta I_L$$

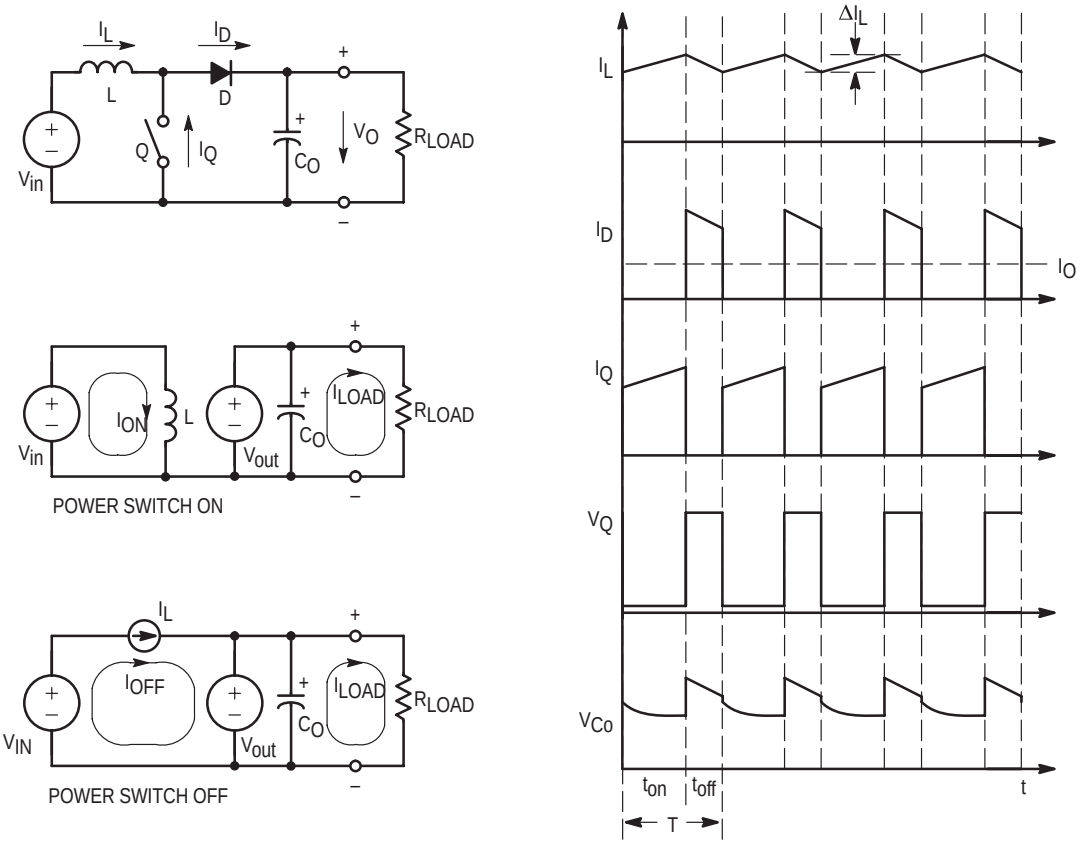

Figure 14. Basic Boost Converter Operation and its Waveforms

5.2.1. Switching Regulator Component Selection

The selection of the external inductor L2 and capacitor C2 values (see Figure 15) is a compromise between the two modes of operation of the switching regulator, the pre regulated voltage VPRE and the dropout voltage of the linear regulators. Ideal equations describing the peak—peak inductor current ripple, peak—peak output voltage ripple and peak inductor current are shown below. Since the switching regulator will work mostly in the buck mode, the inductor and the switcher input and output capacitor were selected for optimum buck controller performance, but also taking into account the restriction placed by adopting the boost converter as well.

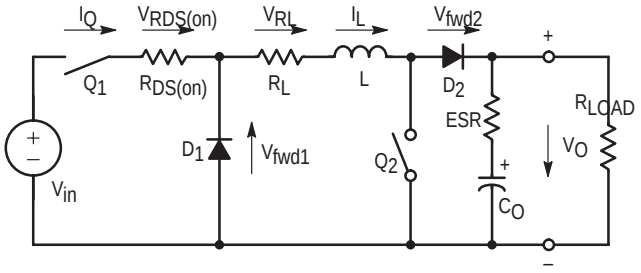

Figure 15. 33394 Switcher Topology

The following example shows a procedure for determining the component values. The VPRE output is set to regulate to 5.6 V and the linear regulators require a minimum of 0.4 V dropout voltage. This leaves a ±0.2 V window for the peak—to–peak output voltage ripple. Assuming the following conditions:

V_{in}(typ) = 13.5 V

I_o = 1.2

VPRE = 5.6 V (+6 V in the boost mode)

f = 200 kHz

$V_{fwd1} = V_{fwd2}$ = 0.5 V

Maximum allowed output voltage ripple in the buck mode $V_{pp(max)}$ = 0.2 V/2 = 0.1 V (to allow for process and temperature variations).

5.2.1.1. Selecting the Inductor

In order to select the proper inductance value, the inductor ripple current ΔI_L has to be determined. The usual ratio of ΔI_L to output current I_o is:

$\Delta I_L = 0.3\ I_o$

As described in the previous section, and taking into account the 33394 switcher topology (see Figure 15), the inductor ripple current can be estimated as:

$$\Delta I_L = \frac{(V_{in} - V_o - V_{fwd2})}{L} \times \frac{V_o + V_{fwd2}}{V_{in} \times f}$$

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After substitution, the calculated inductance value is L = 45 µH, which gives 47 µH standard component value.

The peak–to peak ripple current value is: ΔI_L = 0.345 A.

The peak inductor current is given by:

$I_{Lpk} = 0.5\Delta I_L + I_o = 0.5x0.345 + 1.2 = 1.37[A]$

The inductor saturation current is given by the upper value of the 33394 internal switch current limit $I_{lim(max)}$ = 3.0 A.

Considering also the inductor serial resistance, these requirements are met, for example by the PO250.473T inductor from Pulse Engineering, Inc.

5.2.1.2. Selecting the Catch Diode D_1

The rectifier D_1 current capability has to be greater than calculated average current value.

The maximum reverse voltage stress placed upon this rectifier D_1 is given by maximum input voltage (maximum transient battery voltage). These requirements are met, for example by the HSM350 (3 A, 50 V) schottky diode from Microsemi, Inc.

5.2.1.3. Selecting the Output Capacitor

The output capacitor C_o should be a low ESR part, therefore the 100 µF tantalum capacitor with 80 mΩ ESR was chosen.

From the formula for calculating the ripple voltage:

$V_{ppESR} = \Delta I_L \times R_{ESR} = 0.345 \times 0.08 = 28$ [mV]

One device that meets both, the low ESR, and the temperature stability requirements is, for example, the TPSV107K020R0085 tantalum capacitor from AVX Corp.

Boost Converter Power Capability

The boost converter with selected components has to be able to deliver the required power.

Due to the nature of this non–compensated PFM control technique, the Boost converter output ripple voltage is higher than if it utilized a typical PWM control method. Therefore the switcher output voltage level is set higher than in the Buck mode (in the Boost mode VPRE = +6 V), in order to maintain a sufficient dropout voltage for the 5–volt linear regulators (VDDH, VREFs) and to avoid unwanted Resets to the microcontroller.

The most stringent conditions for the 33394 boost converter occur with the lowest input voltage:

$V_{in(min)}$ = 3.5 V

I_o = 0.8 A

Vpre = +6 V

f = 200 kHz

$V_{fwd1} = V_{fwd2}$ = 0.5 V

d = 0.75, duty cycle is fixed at 75% in boost mode

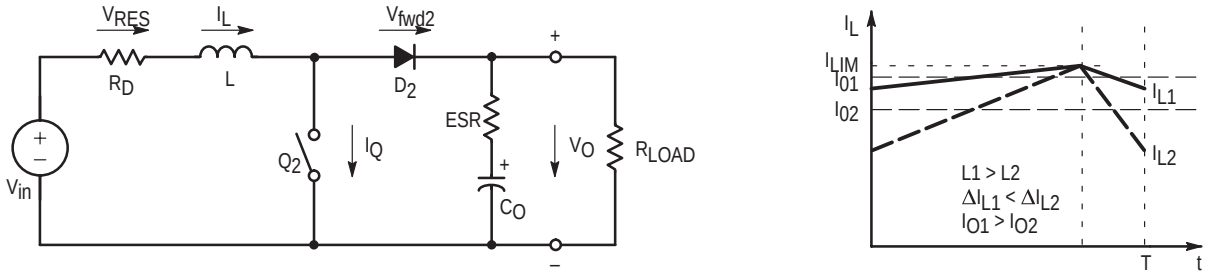

Figure 16. 33394 Switcher Topology – Boost Mode

The input voltage drop associated with the resistance of the internal switch Q1 and inductor series resistance can be estimated as:

$$V_D \approx I_{pk(min)} \times R_D = 2.5\ A \times 0.35\ \Omega = 0.875\ V$$

Where:

V_D is the voltage dissipated on the major parasitic resistances, R_{DSon} of the internal power switch and inductor series resistance R_L.

For the worst case conditions:

$R_D = R_{DSon(max)} + R_L = 0.25 + 0.1 = 0.35[\Omega]$

$I_{pk(min)}$ is the minimum internal power switch current limit value.

Then the equation for calculating ΔI_L can be modified as follows:

$$\Delta I_L = \frac{V_{in} - V_D}{L} \times \frac{[(V_o + V_{fwd2}) - (V_{in} - V_D)] \times d}{(V_o + V_{fwd2}) \times f} =$$

$$= \frac{3.5 - 0.875}{47 \times 10^{-6}} \times \frac{[(6 + 0.5) - (3.5 - 0.875)] \times 0.75}{(6 + 0.5) \times 0.2 \times 10^6}$$

$$= 125[mA]$$

Then the maximum average input current can be calculated as:

$$I_{inAve} = I_{pk(min)} - \frac{1}{2}\Delta I_L = 2.5 - \frac{0.125}{2} = 2.43[A]$$

Finally, the boost converter power capability has to be higher than the required output power or:

$$P_{in(max)} \times \eta > P_{out}$$

Where $P_{in(max)}$ is the boost converter maximum input power:

h is the boost converter efficiency, in our case h is estimated to be h = 85%, and includes switching losses of the external power switch Q2 (MOSFET) inductor and capacitors AC losses, and output rectifier D2 (schottky) switching losses.

P_{out} is the boost converter output power, which includes power loss of the output rectifier D2:

$$P_{out} = (V_o + V_{fwd2}) \times I_o = (6 + 0.5) \times 0.8 = 5.2[W]$$

$$P_{in} = (V_{in} - V_D) \times I_{inAve} \times \eta =$$

$$= (3.5 - 0.875) \times 2.43 \times 0.85 = 5.42[W]$$

As can be seen, the boost converter input power capability meets the required criteria.

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5.2.1.4. Selecting the Power MOSFET Q2

The boost converter maximum output voltage plus the voltage drop across the output schottky rectifier D2 gives the MOSFET's maximum drain–source voltage stress:

$BV_{dsQ2}>V_o+V_{fwd2}$ = 6 V+0.5 V, as can be seen, the breakdown voltage parameter is not critical.

The more important in our case is the Q2 current handling capability. The external power MOSFET has to withstand higher currents than the upper current limit of the 33394:

$I_{DQ2}>3A$

In order to keep the power dissipation of the 33394 boost converter to its minimum, a very low R_{DSon} power MOSFET has to be selected. Moreover, due to the fact that the 33394 external MOSFET gate driver is supplied from VPRE, in order to assure proper switching of Q2 a logic level device has to be selected.

Last but not least, the Q2 package has to suitable for the harsh automotive environment with low thermal resistance.

These requirements are met, for example by the MTD20N03HDL power MOSFET from ON Semiconductor.

5.2.1.5. Selecting the Boost Converter Output Rectifier D2

Criteria similar to that of selecting the power MOSFET was used to select the boost converter output rectifier. Its reverse breakdown voltage is not a critical parameter:

$V_{rD2}>V_o$=6 V

The D2 rectifier has to withstand higher peak current than is the 33394 internal switch upper current limit $I_{lim(max)}$.

The most important parameter is its forward voltage drop, which has to be minimal. This parameter is also crucial for the proper 33394 switcher functionality, and especially for proper transition between the buck and boost modes.

Finally, its switching speed, forward and reverse recovery parameters play a significant role when selecting the output rectifier D2.

These requirements are met, for example by the HSM350 schottky rectifier from Microsemi, Inc.

5.2.2. Input Filter Selection

Since the switcher will work in the Boost mode only during cold crank condition, the 33394 EMC (electromagnetic compatibility) performance is not of concern during this mode of operation. Therefore, only the Buck mode of operation is important for selecting the appropriate input filter. For the Buck converter topology (see Figure 13) the low impedance 3rd order filter (C3, L2, C4 and C26 in the Application Schematic Diagram Figure 20) offers a good solution. It can be seen from the Buck converter current waveforms that comparatively high current pulses are drawn from the converter's input source. The filter inductance must be kept minimal and the capacitor, which is placed right next to the power switch, must be sized large enough to provide sufficient energy reservoir for proper switcher operation.

The ESR of this input capacitor combination C4, C26 has to be sufficiently low to reduce the switching ripple of the switcher input node VBAT. There are three main reasons to keep the voltage ripple of the VBAT pin at its minimum. First, it is the EMC (electromagnetic compatibility) performance of the switcher in the normal operating mode (buck mode). Second, it allows a smooth transition between the boost and buck mode of operation. Third, it helps to avoid entering an undervoltage condition too early. A practical way to achieve sufficiently low ESR of the switcher input capacitor, even at low temperature extremes, is to use several high value ceramic capacitors in parallel with a large electrolytic capacitor. These capacitors should be physically placed as close to the VBAT pins as possible.

5.2.3. Buck Converter Feedback Compensation

A typical control loop of the buck regulator is shown in Figure 17. The loop consists of a power processing block — the modulator in series with an error–detecting block — the Error (Feedback) Amplifier. In principle, a portion of the output voltage (VPRE of the 33394 switcher) is compared to a reference voltage (V_{bg}) in the Error Amplifier and the difference is amplified and inverted and used as a control input for the modulator to keep the controlled variable (output voltage VPRE) constant.

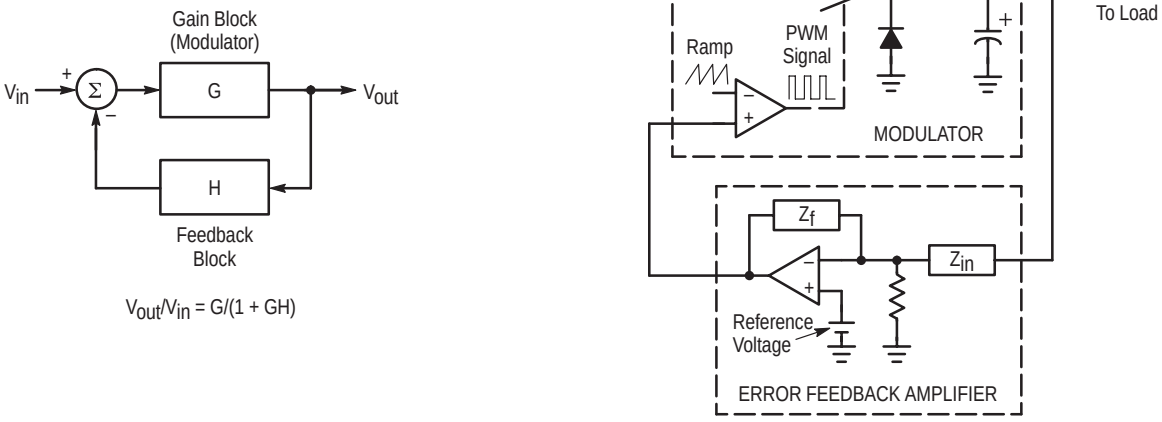

Figure 17. The Buck Converter Control Loop

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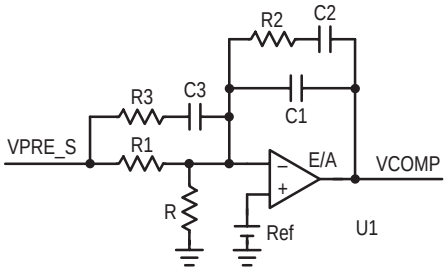

Figure 18. Error Amplifier Two–Pole–Two–Zero Compensation Network

The process of determining the right compensation components starts with analysis of the open loop (modulator) transfer function, which has to be determined and plotted into the Bode plot (see Figure 19). The modulator DC gain can be determined as follows:

$$A_{DC} = \frac{V_{in}}{\Delta V_e}$$

Where V_e is the maximum change of the Error Amplifier voltage to change the duty cycle from 0 to 100 percent (V_e = 2.6 V at Vbat =14 V).

As can be seen from Figure 19, the buck converter modulator transfer function has a double complex pole caused by the output L–C filter. Its corner frequency can be calculated as:

$$f_{p(LC)} = \frac{1}{2\pi\sqrt{LC_O}}$$

This double pole exhibits a —40dB per decade rolloff and a —180 degree phase shift.

Another point of interest in the modulator's transfer function is the zero caused by the ESR of the output capacitor C_O and the capacitance of the output capacitor itself:

$$f_{z(ESR)} = \frac{1}{2\pi R_{ESR} C_O}$$

The ESR zero causes +20dB per decade gain increase, and +90 degree phase shift.

Once the open loop transfer function is determined, the appropriate compensation can be applied in order to obtain the required closed loop cross over frequency and phase margin (~60 degree) — refer to Figure 18 and Figure 19.

Figure 19 shows the 33394 Switching Regulator modulator gain–phase plot, E/A gain–phase plot, closed loop gain–phase plot, and the E/A compensation circuit. The frequency f_{xo} is the required cross–over frequency of the buck regulator.

In order to achieve the best performance (the highest bandwidth) and stability of the voltage–mode controlled buck PWM regulator the two–pole–two–zero type of compensation was selected — see Figure 19 for the compensated Error Amplifier Bode plot, and Figure 18 for the compensation network. The two compensating zeros and their positive phase shift (2 x +90 degree) associated with this type of compensation can counteract the negative phase shift caused by the double pole of the modulator's output filter.

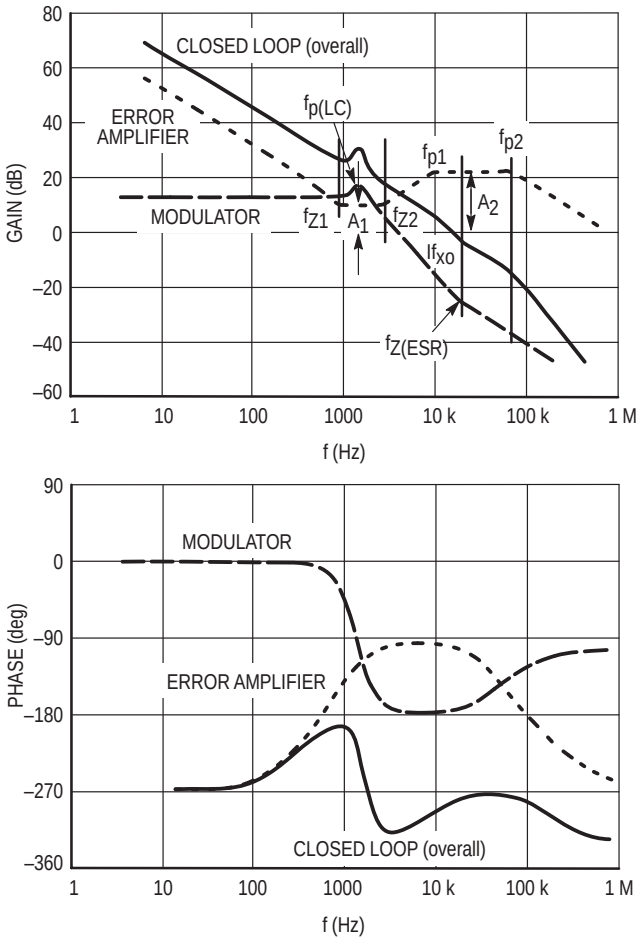

Figure 19. Bode Plot of the Buck Regulator

The frequency of the compensating poles and zeros can be calculated from the following expressions:

$$f_{z1} = \frac{1}{2\pi R_2 C_2}$$

$$f_{z2} = \frac{1}{2\pi(R_1 + R_3)C_3} \approx \frac{1}{2\pi R_1 C_3}$$

$$f_{p1} = \frac{1}{2\pi R_3 C_3}$$

$$f_{p2} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \approx \frac{1}{2\pi R_2 C_1}$$

and the required absolute gain is:

$$A_1 = \frac{R_2}{R_1}$$

$$A_2 = \frac{R_2(R_1 + R_3)}{R_1 R_3} \approx \frac{R_2}{R_3}$$

Refer to Application Schematic Diagram (Figure 20) and Table 2 for the 33394 switcher component values.

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Table 2.

Part number (Figure 18)	Application diagram part number (Figure 1)	Component value
R1	33394 internal resistor	39.6kΩ
R2	R2	100kΩ
R3	R1	430Ω
C1	C6	100pF
C2	C7	1.0nF
C3	C5	3.3nF

5.3. Selecting Pull–Up Resistors

All the Resets (/PORESET, /PRERESET and /HRESET) are open drain outputs, which can sink a maximum of 1 mA drain current. This determines the pull–up resistor minimum value. VKAM should be used as the pull–up source for the /PORESET output. /PORESET is pulled low only during initial battery connect or when VKAM is below 2.5 volts (for VDDL = 2.6 V).

To select the /PRERESET and /HRESET pull–up resistor connections, consider current draw during sleep modes. For example, the pull up resistor on /PRERESET and /HRESET should receive its source from VDDL, if the sleep mode or low power mode of the module is initiated primarily by the state of the VIGN pin. Refer to Figure 20 for recommended pull–up resistor values.

Another way to connect the /PRERESET and /HRESET pull–up resistors is to connect them to the VKAM output together with the /PORESET pull–up resistor (see Figure 1). This is the preferable solution when the sleep or low power mode is initiated primarily by the microprocessor. In that case, when the 33394 is shut down by pulling the /SLEEP pin down, all three Resets (/PORESET, /PRERESET and /HRESET) stay high. Since they are pulled–up to the supply voltage (VKAM) they draw no current from the VKAM and the module quiescent current is minimized.

5.4. Selecting Hardware Reset Timer Components

The HRT input sets the delay time from VDDH, VDD3_3 and VDDL stable to the release of /PRERESET and /HRESET. When sizing the delay time the module design engineer must consider capacitor leakage, printed board leakage and HRT pin leakage. Resistor selection should be low enough to make the leakage currents negligible. The Hardware Reset (/HRESET) delay can be calculated as follows:

Delay time:

$$t_D = -RC \times \ln\left[\frac{(V_B - V_{SAT}) - V_{th}}{(V_B - V_{SAT})}\right]$$

Where R is the HRT timer pull–up resistor,

C is the HRT timer capacitor

V_B is the pull–up voltage,

V_{th} is the HRT timer threshold voltage (V_{th} = 2.5V nominal value),

V_{SAT} is the saturation voltage of the internal pull–down transistor.

If the HRT timer pull–up resistor is connected to VDDH (see Figure 1) and the resistor value is ≥ 47 kΩ, therefore the V_{SAT} can be neglected, the formula for calculating the time delay can be simplified to:

$$t_D = 0.7 \times RC$$

5.5. Selecting the VKAM Resistor Divider

The VKAM linear regulator output voltage is divided by an external resistor divider and compared with the bandgap reference voltage (V_{bg}) in the input of the VKAM error amplifier. The resistor divider can be designed according to the following formula:

$$V_{KAM} = V_{KAMref} \times \left(1 + \frac{R_{upper}}{R_{lower}}\right)$$

V_{KAMref} = 1.267 V

Where V_{KAMref} is the bandgap reference voltage.

Since the VKAM feedback pin (VKAM_FB) input current is only a few nA, the resistor value can be selected sufficiently high in order to minimize the quiescent current of the module. See Figure 20 for the VKAM resistor divider recommended values.

5.6. Selecting the VDDL Resistor Divider

The VDDL regulator resistor divider is designed according to the same formula as described in the paragraph above (see Figure 20).

$$V_{DDL} = V_{DDLref} \times \left(1 + \frac{R_{upper}}{R_{lower}}\right)$$

Where V_{DDLref} = 1.267 V

Nonetheless, the actual resistor values should be chosen several decades lower than in the previous example. This is due to the fact that the VDDL linear regulator needs to be pre–loaded by a minimum of 10 mA current in order to guarantee stable operation. See Figure 20 for the VDDL resistor divider recommended values.

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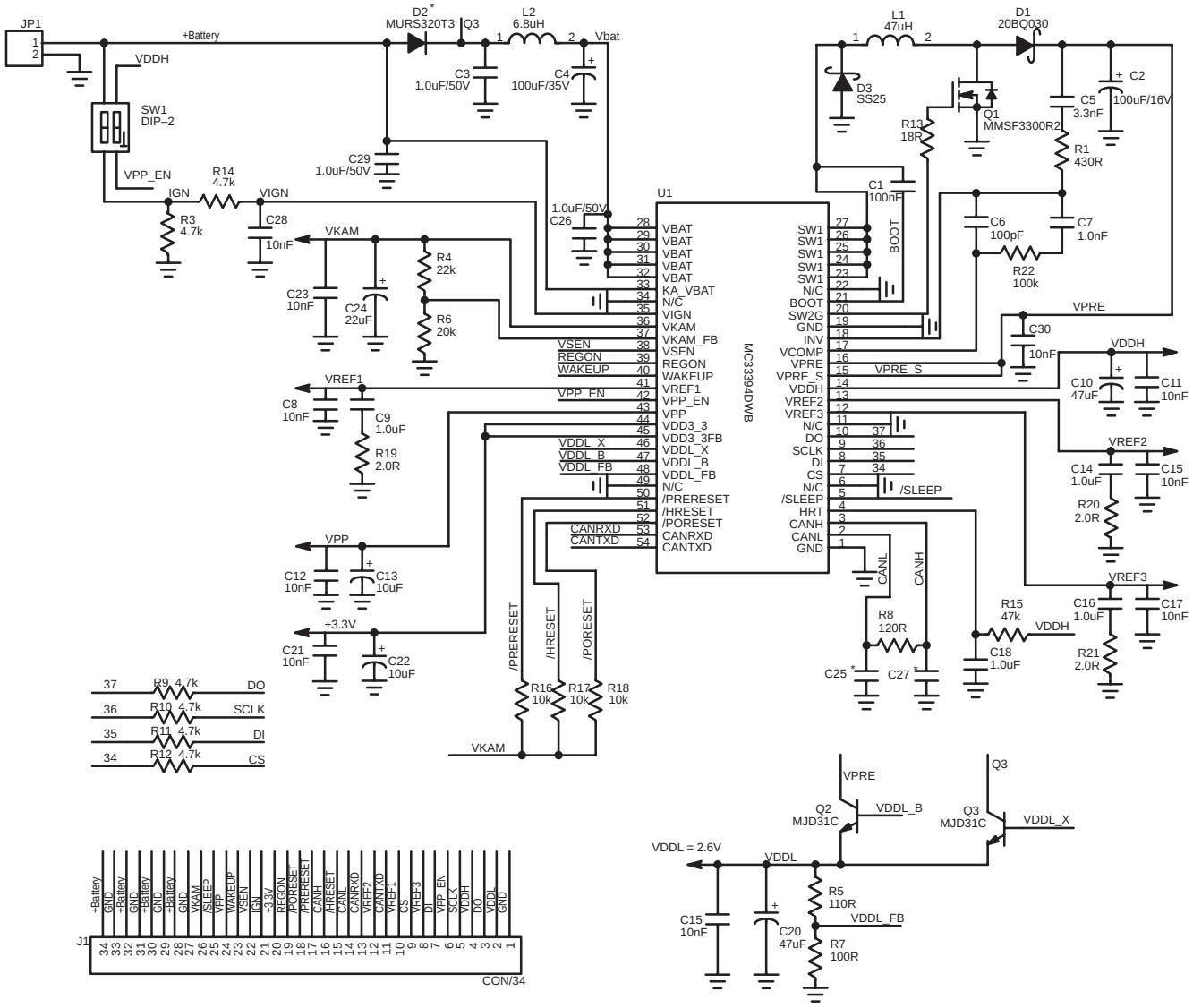

*Notes: 1. D2 is a protection diode against reverse battery fault condition. In those applications, which do not require this type of protection, diode D2 can be ommitted.
2. Capacitors C25, C27 are optional and may be used for CAN tranceiver evaluation.

Figure 20. 33394 Application Circuit Schematic Diagram

Table 3. 33394 Evaluation Board Performance

Parameter	Value (T_A = 25°C, Vin = 14V)		Line Regulation (Vin = 5.2V to 26.5V)		Load Regulation (Vin = 14 V)	
	V [mV]	Load [mA]	ΔV [mV]	Load [mA]	ΔV [mV]	Load [mA]
VDDH	5.028	400	10	400	18	0 to 400
VPP	5.026	150	10	150	5	0 to 150
VREF1	5.023	100	8	100	8	0 to 100
VREF2	5.022	100	8	100	10	0 to 100
VREF3	5.021	100	6	100	11	0 to 100
VDD3_3	3.307	120	5	120	7	0 to 120
VDDL	2.667	400	5	400	10	0 to 400
VKAM	2.638	60	2	60	14	0 to 60

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Table 4. 33394DWB Evaluation Board Bill of Material

Item	Qty.	Part Designator	Value/ Rating	Part Number/ Manufacturer
1	1	C1	100nF/16V, Ceramic X7R	Any manufacturer
2	1	C2	100µF/20V	TPSV107K020R0085, AVX Corp.
3	3	C3,C26,C29	1.0µF/50V	C1812C105K5RACTR, Kemet
4	1	C4	100µF/35V	UUB1V101MNR1GS, Nichicon
5	1	C5	3.3nF, Ceramic X7R	Any manufacturer
6	1	C6	100pF, Ceramic X7R	Any manufacturer
7	1	C7	1.0nF, Ceramic X7R	Any manufacturer
8	10	C8,C11,C12,C15,C17,C19,C21,C23,C28,C30	10nF, Ceramic X7R	Any manufacturer
9	4	C9,C14,C16,C18	1.0µF, Ceramic X7R	Any manufacturer
10	2	C20,C10	47µF/10V, Tantalum	TPSC476K010R0350, AVX Corp.
11	1	C13	10µF/16V, Tantalum	TPSB106K016R0800, AVX Corp.
12	1	C22	10µF/6.3V, Tantalum	TPSA106K006R1500, AVX Corp.
13	1	C24	22µF/6.3V, Tantalum	TPSA226K006R0900, AVX Corp.
14	2	C25,C27	470pF, Ceramic X7R	Any manufacturer
15	1	D1	30V/2A Schottky	20BQ030, International Rectifier
16	1	D2	200V/3A Diode	MURS320T3, ON Semiconductor
17	1	D3	50V/2A Schottky	SS25, General Semiconductor
18	1	JP1	2–pin, 0.2 (5.1mm)	Terminal Block
19	1	J1	34–pin, 0.1 x 0.1	PCB Header Connector
20	1	L1	47µH	P0250.473T, Pulse Engineering
21	1	L2	6.8µH	P0751.682T, Pulse Engineering
22	1	Q1	30V/11.5A, Mosfet	MMSF3300R2, ON Semiconductor
23	2	Q2,Q3	100V/3A, BJT	MJD31C, ON Semiconductor
24	1	R1	430R, Resistor 0805	Any manufacturer
25	1	R2	100k, Resistor 0805	Any manufacturer
26	6	R3,R9,R10,R11,R12,R14	4.7k, Resistor 0805	Any manufacturer
27	1	R4	22k, Resistor 0805, 1%	Any manufacturer
28	1	R5	110R, Resistor 0805, 1%	Any manufacturer
29	1	R6	20k, Resistor 0805, 1%	Any manufacturer
30	1	R7	100R, Resistor 0805, 1%	Any manufacturer
31	1	R8	120R, Resistor 0805	Any manufacturer
32	1	R13	18R, Resistor 0805	Any manufacturer
33	1	R15	47k, Resistor 0805	Any manufacturer
34	3	R16,R17,R18	10k, Resistor 0805	Any manufacturer
35	3	R19,R20,R21	2.0R, Resistor 0805	Any manufacturer
36	1	SW1	2–Position DIP Switch	BD02, C&K Components
37	1	TP1	Test Point, 0.038	240–333, Farnell
38	1	U1	Integrated Circuit	33394DWB/ Motorola

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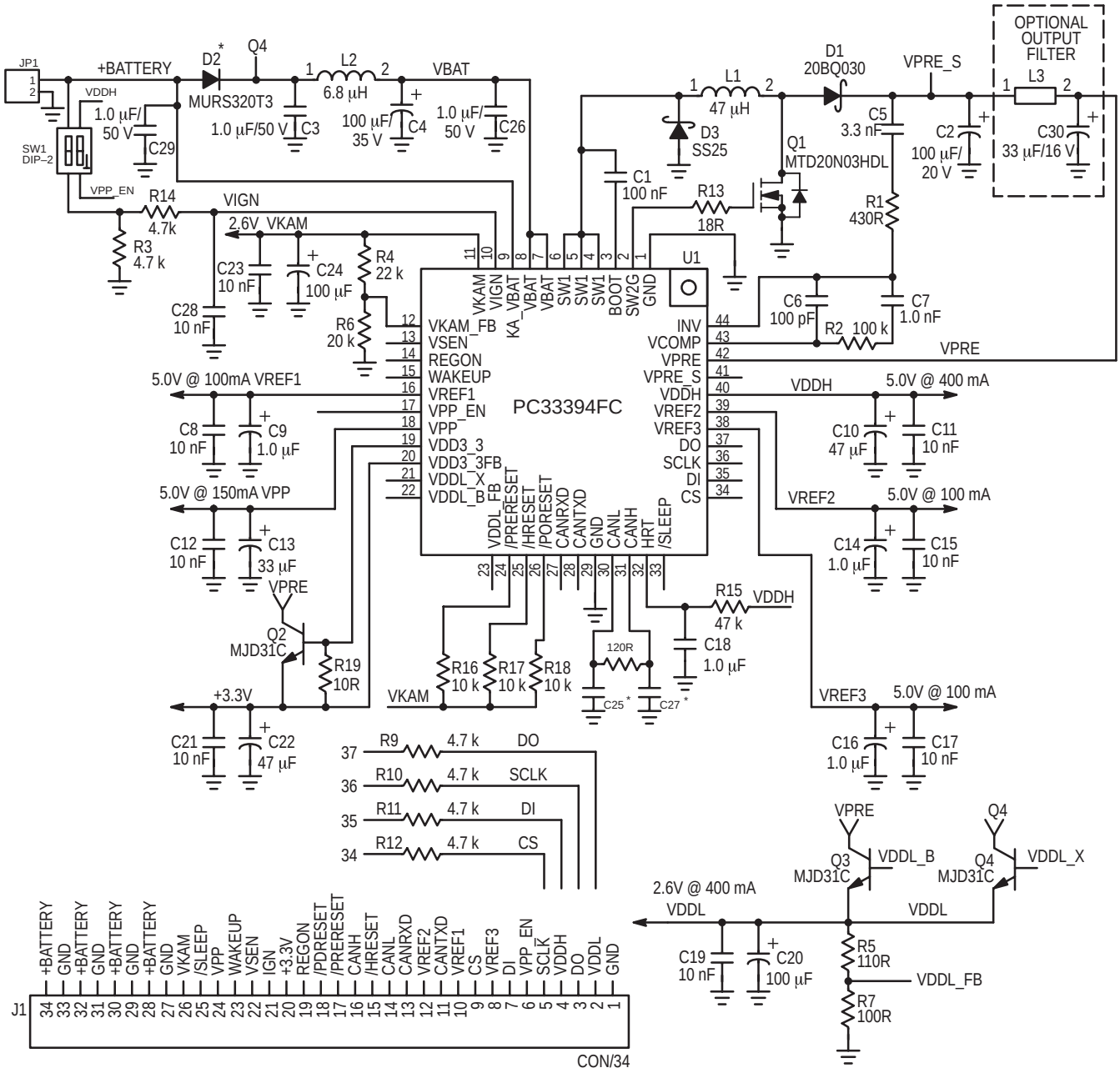

*Notes: 1. D2 is a protection diode against reverse battery fault condition. In those applications, which do not require this type of protection, diode D2 can be ommitted.
2. Capacitors C25, C27 are optional and may be used for CAN tranceiver evaluation.

Figure 21. 33394 Application Circuit with Increased 3.3V Output Current Capability

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Table 5. 33394FC Evaluation Board Bill of Material

Item	Qty.	Part Designator	Value/ Rating	Part Number/ Manufacturer
1	1	C1	100nF/16V, Ceramic X7R	Any manufacturer
2	1	C2	100µF/20V	TPSV107K020R0085, AVX Corp.
3	3	C3,C26,C29	1.0µF/50V	C1812C105K5RACTR, Kemet
4	1	C4	100µF/35V	UUB1V101MNR1GS, Nichicon
5	1	C5	1.5nF, Ceramic X7R	Any manufacturer
6	1	C6	100pF, Ceramic X7R	Any manufacturer
7	1	C7	1.0nF, Ceramic X7R	Any manufacturer
8	9	C8,C11,C12,C15,C17,C19,C21,C23,C28	10nF, Ceramic X7R	Any manufacturer
9	1	C18	1.0µF, Ceramic X7R	Any manufacturer
10	3	C9,C14,C16	1.0µF/35V Tantalum	TPSA105K035R3000, AVX Corp.
11	2	C10,C22	47µF/10V Tantalum	TPSC476K010R0350, AVX Corp.
12	1	C13	33µF/10V Tantalum	TPSB336K010R0500, AVX Corp.
13	1	C20	100µF/6.3V Tantalum	TPSC107K006R0150, AVX Corp.
14	1	C24	22µF/6.3V, Tantalum	TPSA226K006R0900, AVX Corp.
15	2	C27,C25	470pF, Ceramic X7R	Any manufacturer
16	1	C30	33µF/16V	TPSC336K016R0300, AVX Corp.
17	1	D1	30V/ 2A Schottky	20BQ030, International Rectifier
18	1	D2	200V/3A Diode	MURS320T3, ON Semiconductor
19	1	D3	SS25	SS25, General Semiconductor
20	1	JP1	2–pin, 0.2 (5.1mm)	Terminal Block
21	1	J1	34–pin, 0.1 x 0.1	PCB Header Connector
22	1	L1	47µH	P0250.473T, Pulse Engineering
23	1	L2	6.8µH	P0751.682T, Pulse Engineering
24	1	L3	Ferrite Bead	HF30ACC575032/ TDK
25	1	Q1	30V/20A Mosfet	MTD20N03HDL, ON Semiconductor
26	3	Q2,Q3,Q4	100V/3A BJT	MJD31C, ON Semiconductor
27	1	R1	680R, Resistor 0805	Any manufacturer
28	1	R2	100k, Resistor 0805	Any manufacturer
29	6	R3,R9,R10,R11,R12,R14	4.7k, Resistor 0805	Any manufacturer
30	1	R4	22k, Resistor 0805, 1%	Any manufacturer
31	1	R5	110R, Resistor 0805, 1%	Any manufacturer
32	1	R6	20k, Resistor 0805, 1%	Any manufacturer
33	1	R7	100R, Resistor 0805, 1%	Any manufacturer
34	1	R8	120R, Resistor 0805	Any manufacturer
35	1	R13	18R, Resistor 0805	Any manufacturer
36	1	R15	47k, Resistor 0805	Any manufacturer
37	3	R16,R17,R18	10k, Resistor 0805	Any manufacturer
38	1	R19	10R, Resistor 0805	Any manufacturer
39	1	SW1	2–Position DIP Switch	BD02, C&K Components
40	1	TP1	Test Point	240–333, Farnell
41	1	U1	Integrated Circuit	MC33394DWB/ Motorola

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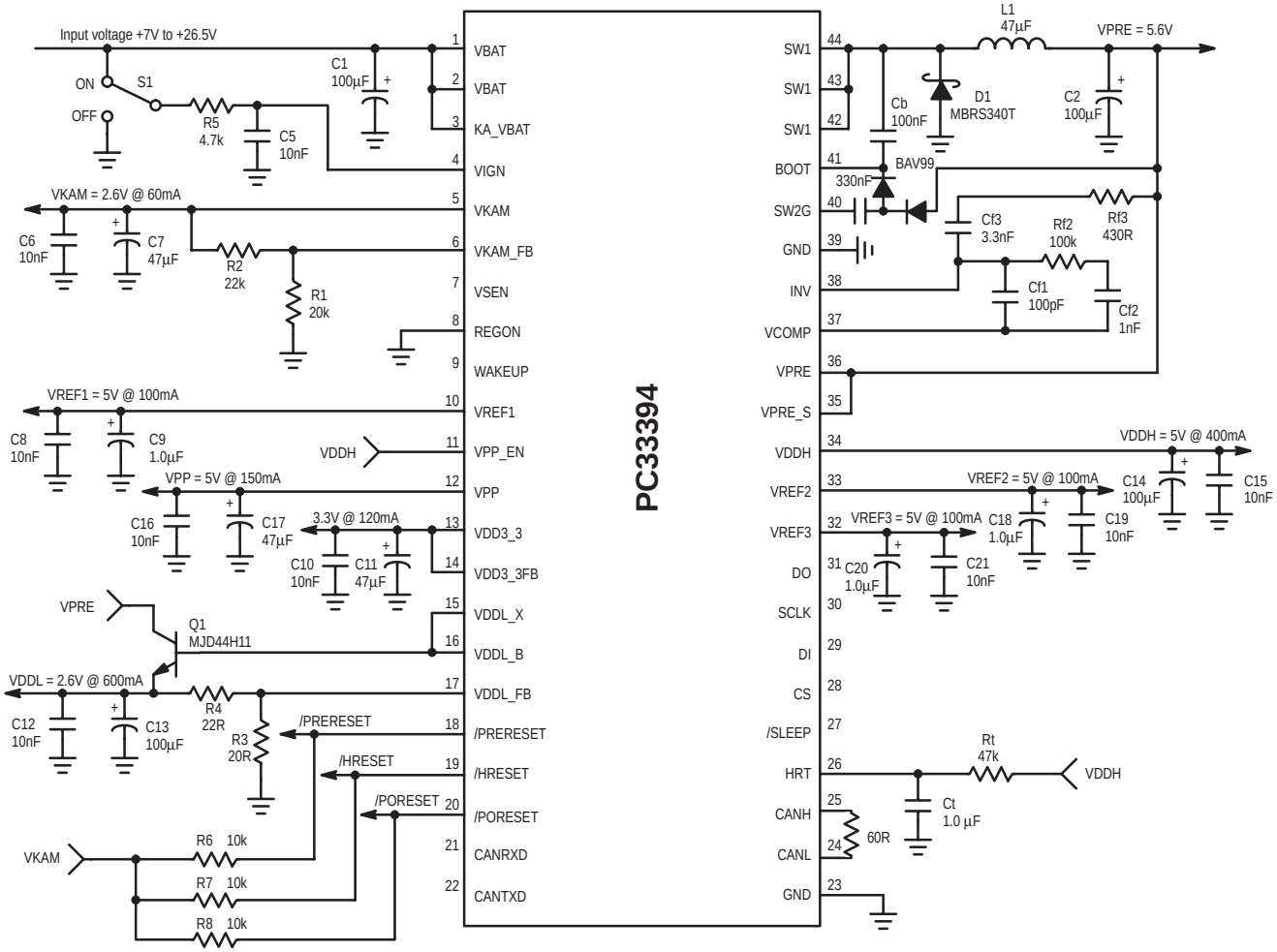

Figure 22. 33394 Buck–Only Application

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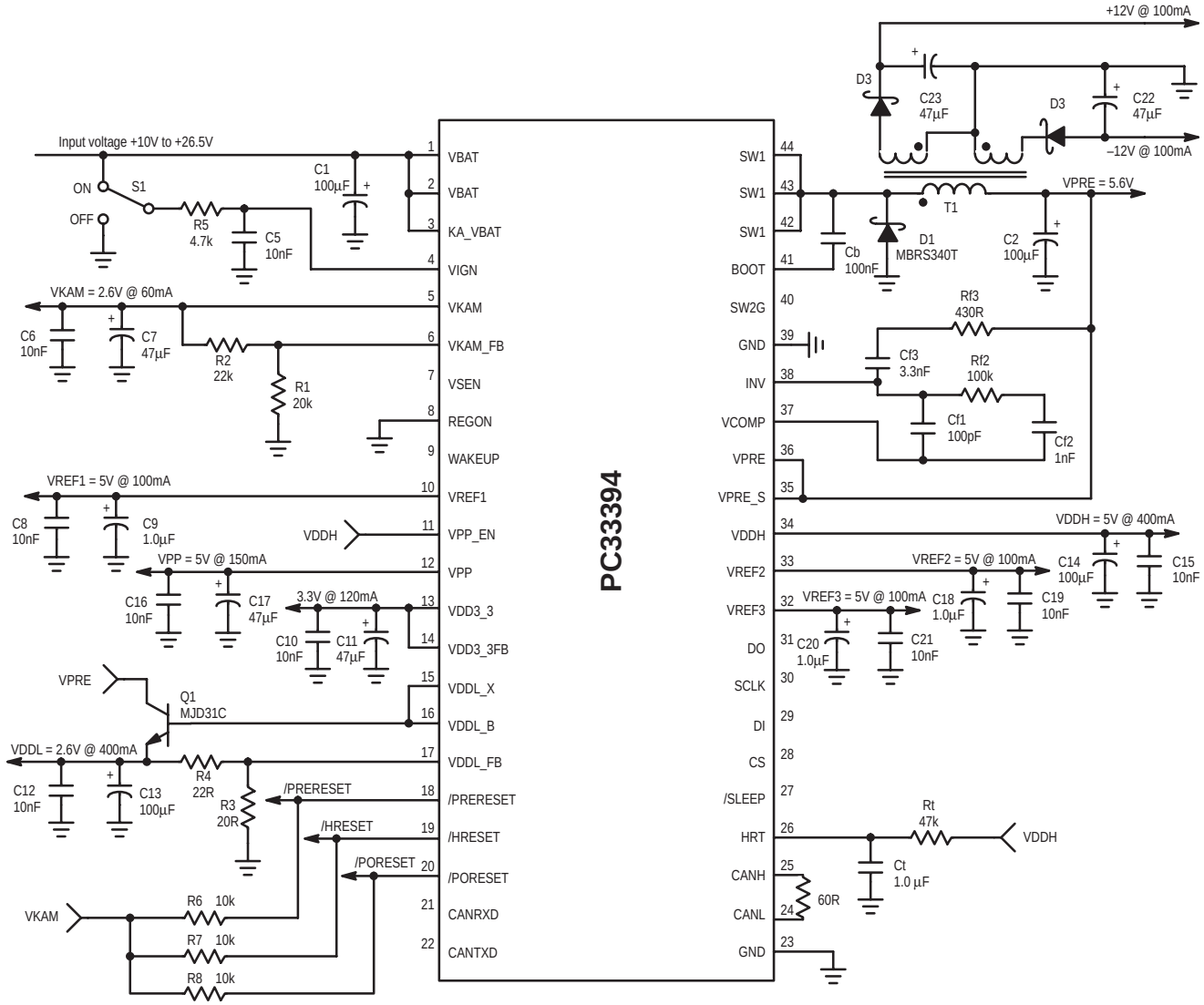

Figure 23. 33394 Flyback Converter Provides Symmetrical Voltages

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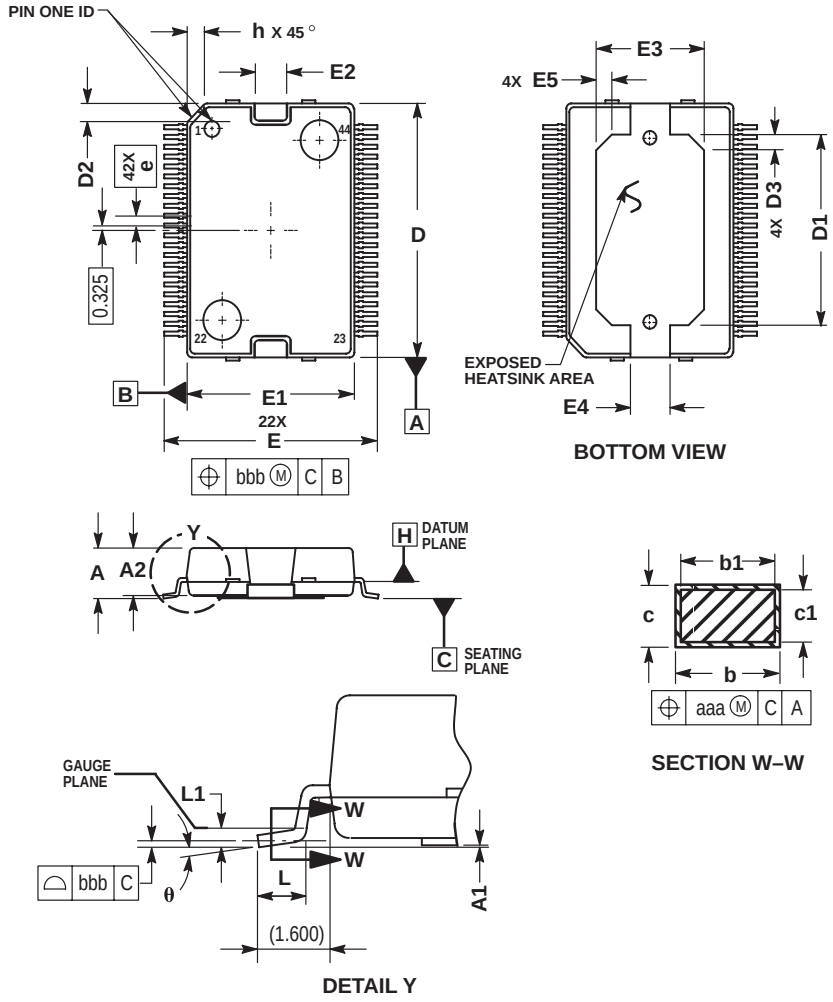
PACKAGE DIMENSIONS

DH SUFFIX
44–LEAD HSOP
PLASTIC PACKAGE
CASE 1291–01
ISSUE O



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.025	0.125
A2	2.900	3.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
D3	—	1.000
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.300
E4	2.700	2.900
E5	—	1.000
L	0.840	1.100
L1	0.350 BSC	
b	0.220	0.350
b1	0.220	0.320
c	0.230	0.320
c1	0.230	0.280
e	0.650 BSC	
h	—	0.800
θ	0 °	8 °
aaa	0.200	
bbb	0.100	

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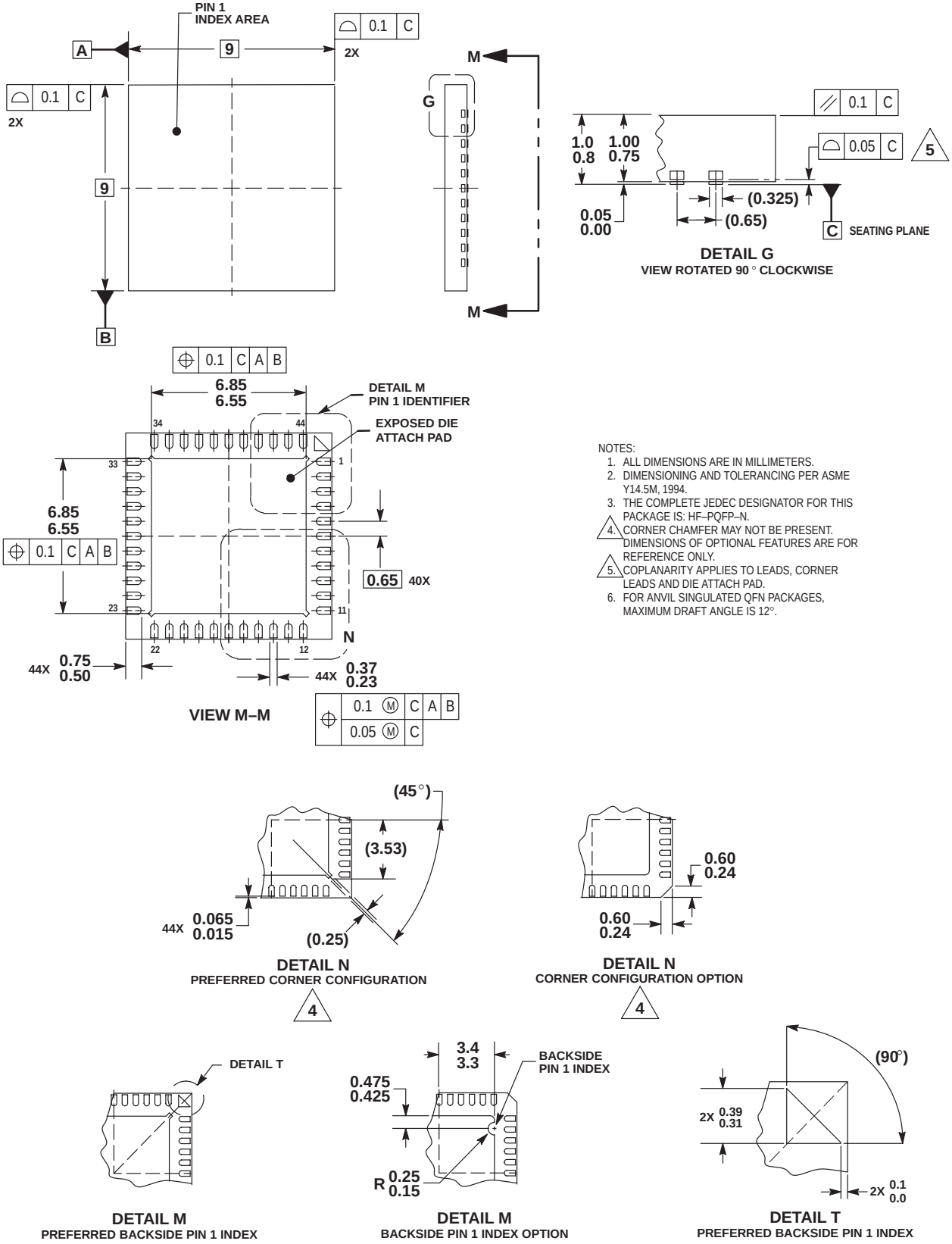
PACKAGE DIMENSIONS

FC SUFFIX
44–LEAD QFN
PLASTIC PACKAGE
CASE 1310–01
ISSUE D



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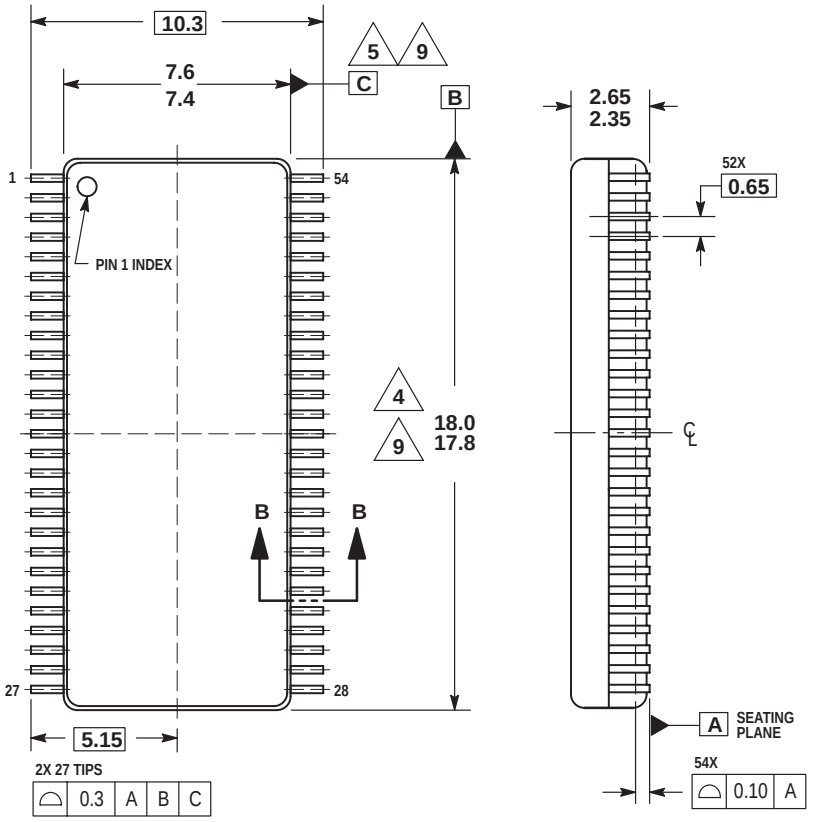
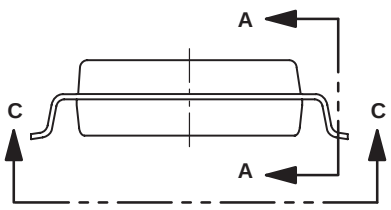
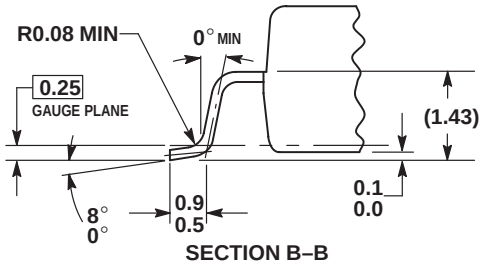
PACKAGE DIMENSIONS

DWB SUFFIX
54–LEAD SOICW–EP
PLASTIC PACKAGE
CASE 1377–01
ISSUE B

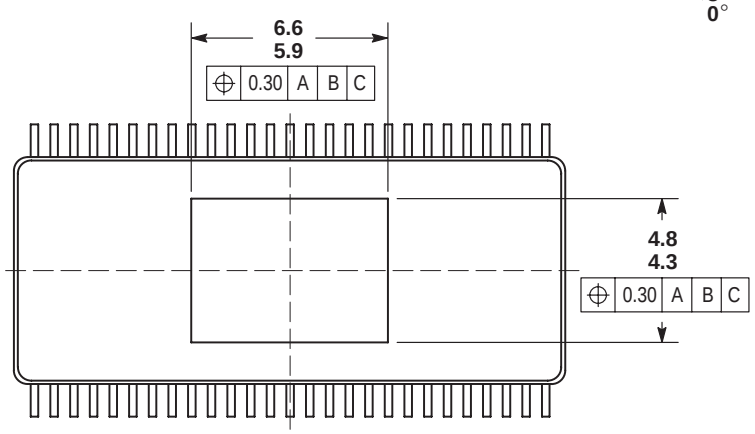


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

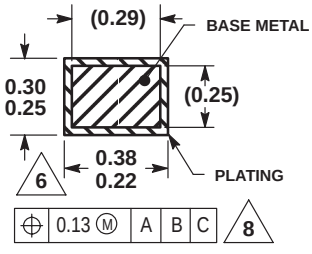




SECTION B–B



VIEW C–C



SECTION A–A
ROTATED 90° CLOCKWISE

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NOTES

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NOTES

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